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United States Patent [19]

Ishihara et al.

[11] Patent Number: 5,448,379

[45] Date of Patent: Sep. 5, 1995

[54] METHOD AND APPARATUS FOR FORMING COLOR IMAGES BY CONVERTING A COLOR SIGNAL TO A FURTHER COLOR DENSITY SIGNAL

[75] Inventors: Hideshi Ishihara, Katano; Haruo Yamashita, Osaka; Yasuki Matsumoto, Takarazuka, all of Japan

[73] Assignee: Matsushita Electric Industrial Co., Ltd., Kadoma, Japan

[21] Appl. No.: 77,930

[22] Filed: Jun. 18, 1993

[30] Foreign Application Priority Data

Jun. 19, 1992 [JP] Japan 4-160757
Nov. 25, 1992 [JP] Japan 4-313849

[51] Int. Cl.[6] G03F 3/08; H04N 1/46

[52] U.S. Cl. 358/518; 358/523; 358/515; 358/504

[58] Field of Search 358/500, 518, 517, 523, 358/525, 515, 504

[56] References Cited

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Primary Examiner—Edward L. Coles, Sr.
Assistant Examiner—Allan A. Esposo
Attorney, Agent, or Firm—Willian Brinks Hofer Gilson & Lione

[57] ABSTRACT

Method and apparatus for forming color images on paper using a sublimation type thermal transfer full-color printer using three color inks of yellow, magenta, and cyan. A color input signal to be printed is subjected to a first color correction process. The first color correction process performs a color correction using linear and non-linear masking operations and produces first ink-density signals. The first ink-density signals are judged for reproducibility by the printer by determining whether the signals fit within a gamut of colors. If judged to be reproducible, the first ink-density signals are passed on to the printer. However, if the first ink-density signals are judged to be outside the gamut of colors, the signals are subjected to a second correction process. The second color correction process first obtains a target color for color reproduction by the printer. Next, the second process sets ink-density signals, obtains predicted colors realized by the ink-density signals, chooses an output ink-density signal such that an evaluation value calculated by the target color and the predicted color becomes minimal, and produces a second ink-density signal that results in optimal colors within the range of colors reproducible by the printer.

7 Claims, 17 Drawing Sheets

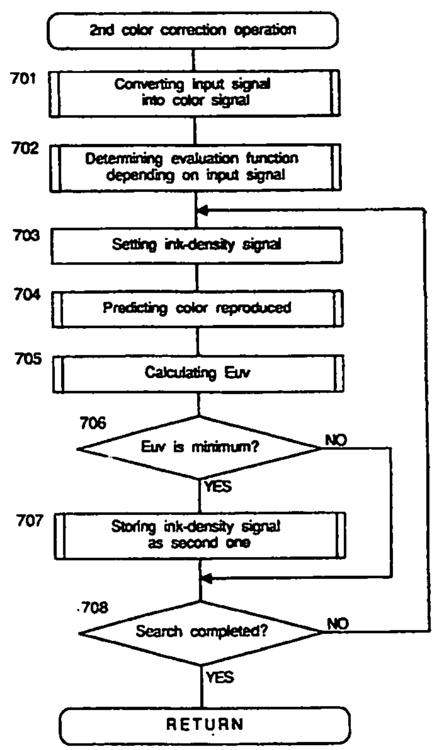


Fig.1

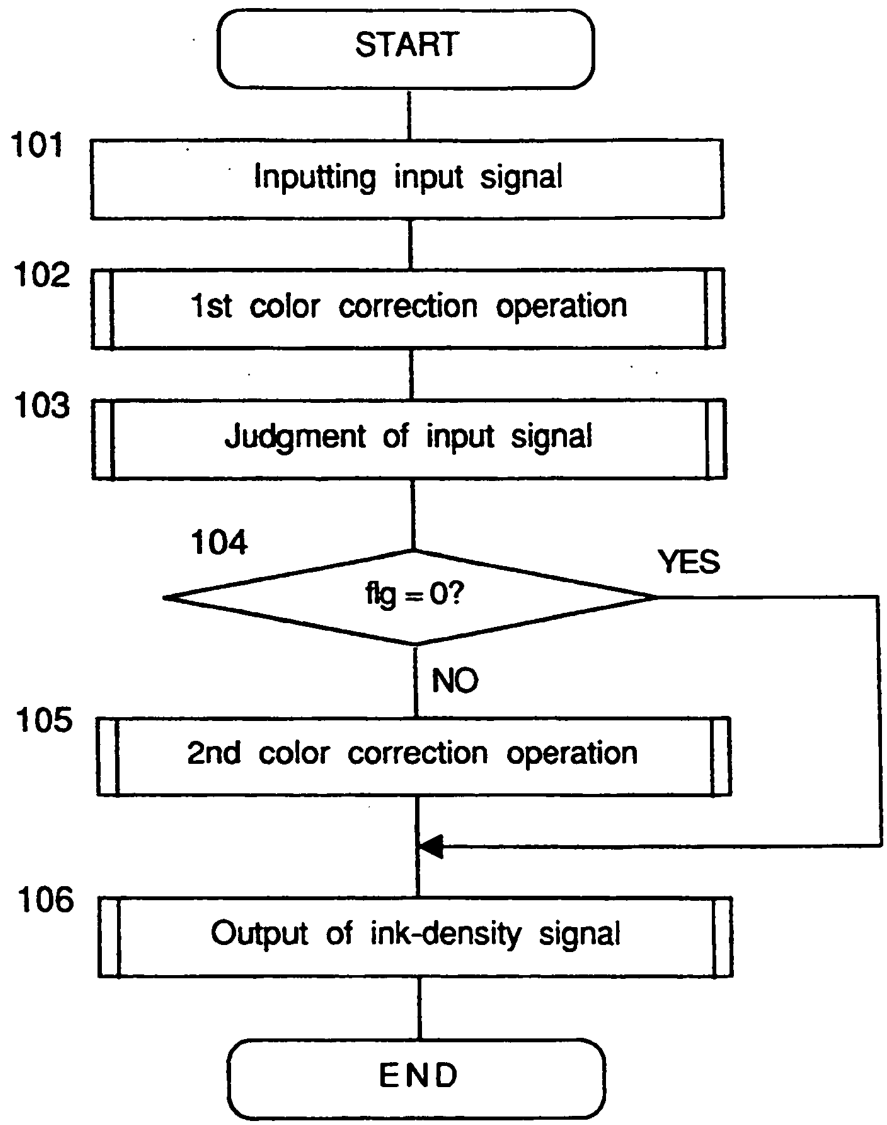

START
101
Inputting input signal
102
1st color correction operation
103
Judgment of input signal
104
flg = 0?
YES
NO
105
2nd color correction operation
106
Output of ink-density signal
END

Fig.2

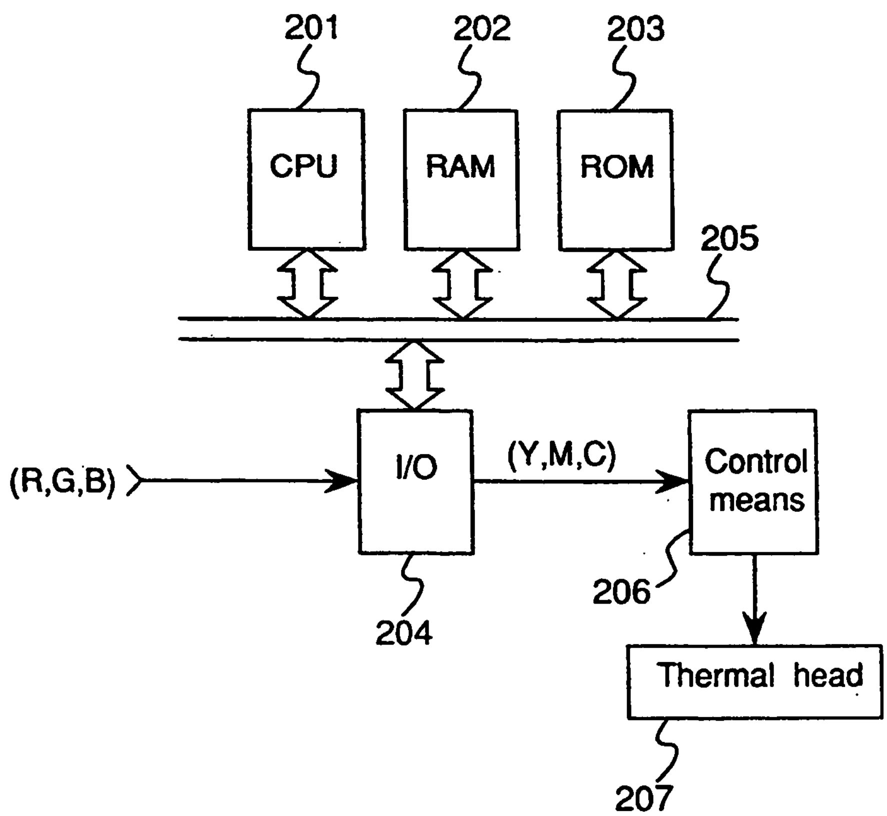

201
202
203
CPU
RAM
ROM
205
(R,G,B)
I/O
(Y,M,C)
Control means
206
204
Thermal head
207

Fig.3

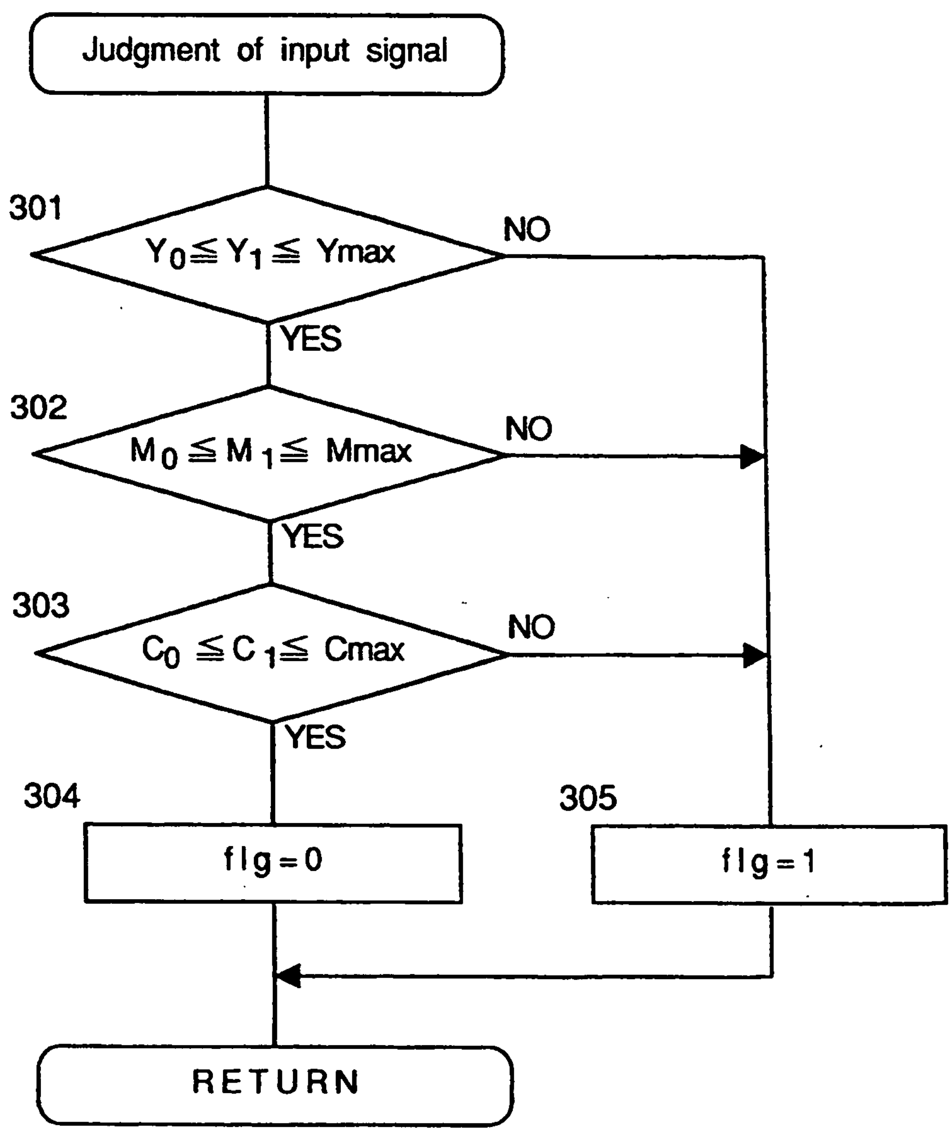

Judgment of input signal
301
$Y_0 \leqq Y_1 \leqq Ymax$
NO
YES
302
$M_0 \leqq M_1 \leqq Mmax$
NO
YES
303
$C_0 \leqq C_1 \leqq Cmax$
NO
YES
304
flg=0
305
flg=1
RETURN

Fig. 4(a)

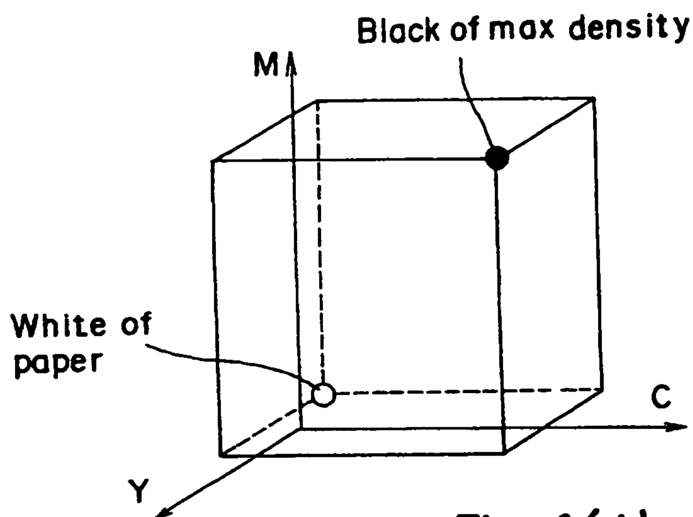


Fig. 4(b)

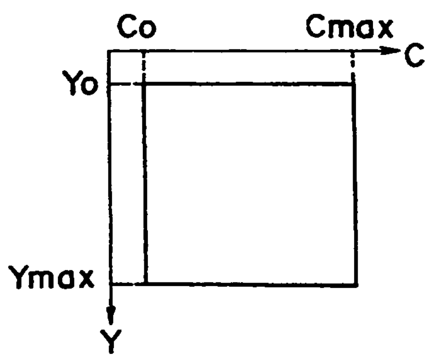


Fig. 4(c)

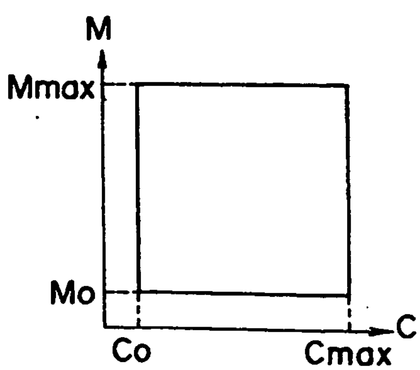


Fig. 4(d)

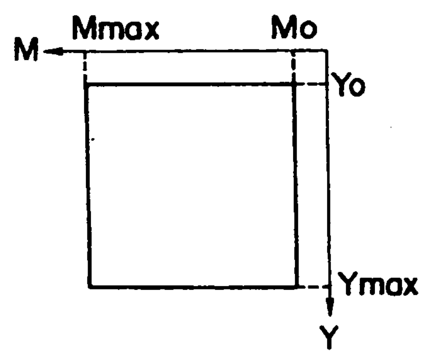


Fig.5

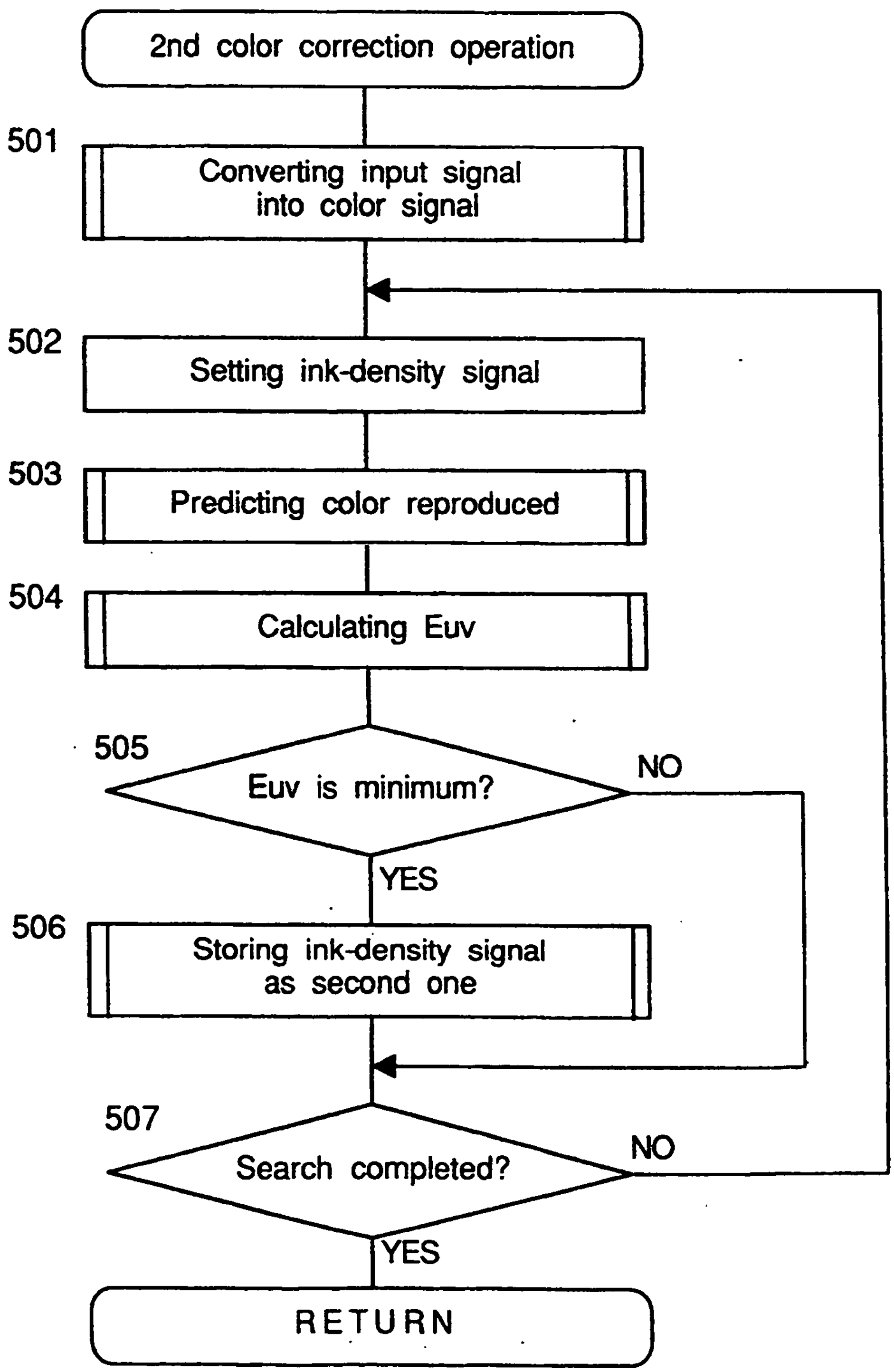

2nd color correction operation
501
Converting input signal into color signal
502
Setting ink-density signal
503
Predicting color reproduced
504
Calculating Euv
505
Euv is minimum?
NO
YES
506
Storing ink-density signal as second one
507
Search completed?
NO
YES
RETURN

Fig. 6(a)

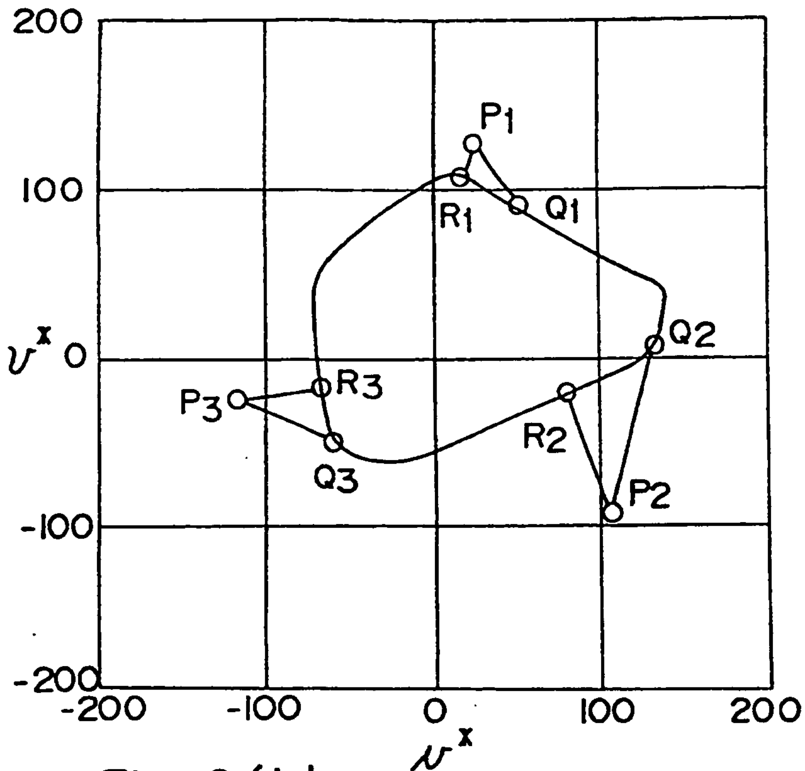


Fig. 6(b)

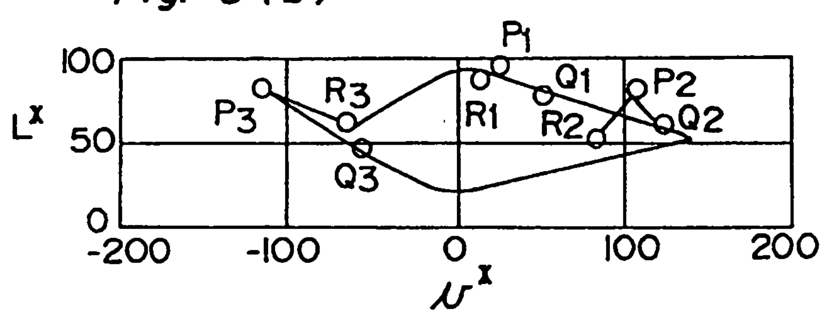


Fig. 6(c)

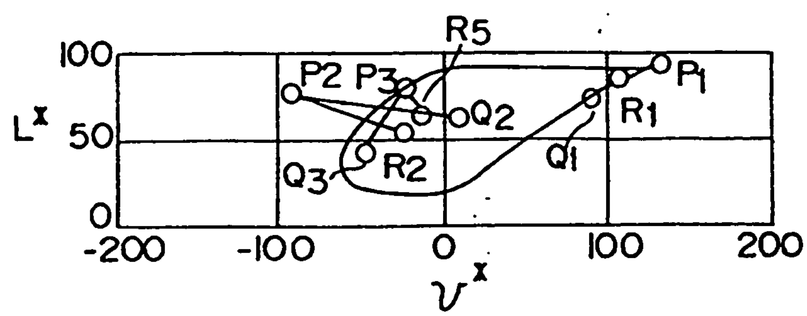


Fig. 7

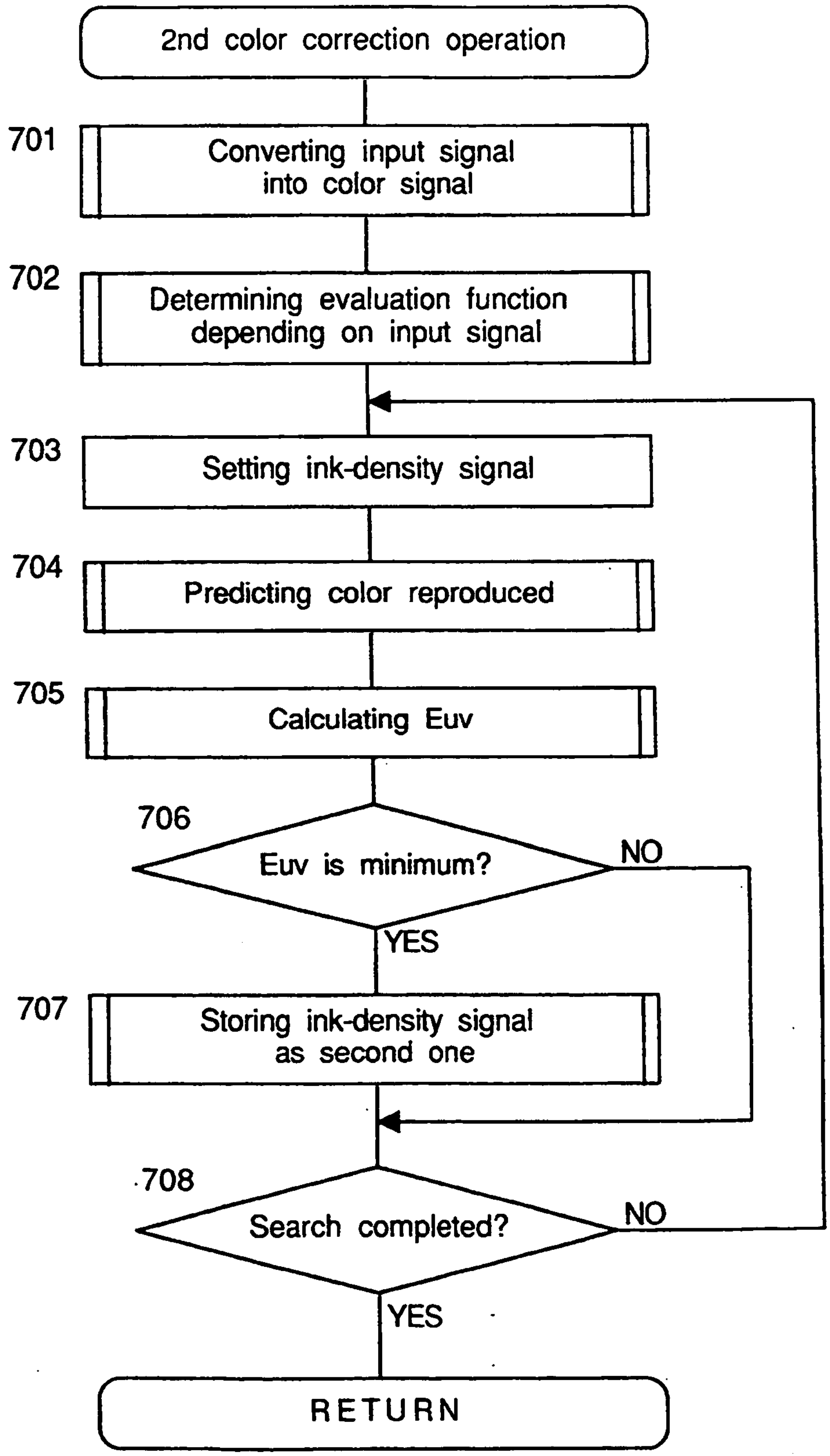

2nd color correction operation
701
Converting input signal into color signal
702
Determining evaluation function depending on input signal
703
Setting ink-density signal
704
Predicting color reproduced
705
Calculating Euv
706
Euv is minimum?
NO
YES
707
Storing ink-density signal as second one
708
Search completed?
NO
YES
RETURN

Fig. 8 (a)

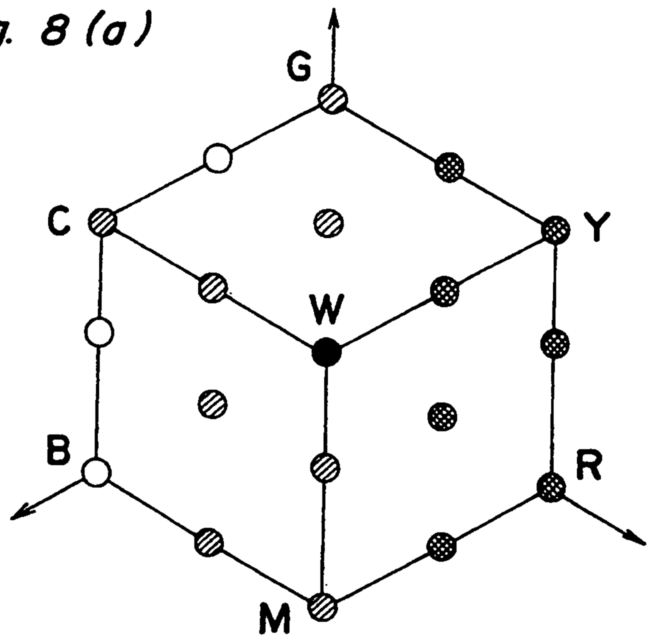

G
C
Y
W
B
R
M

Fig. 8 (b)

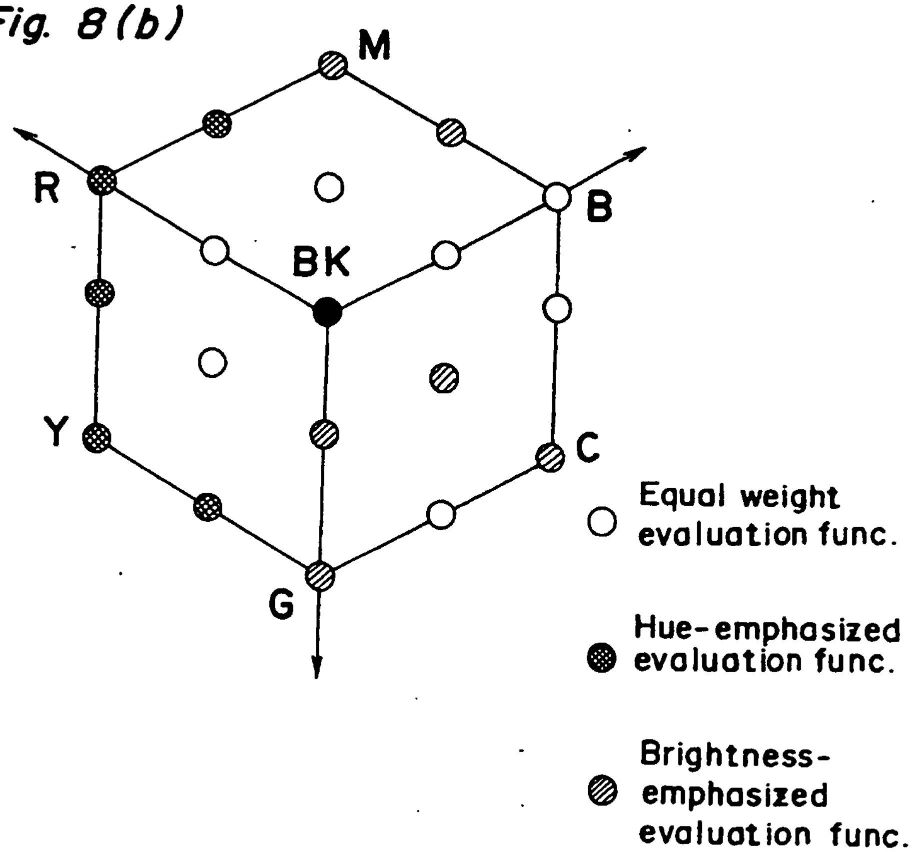

M
R
B
BK
Y
C
G
Equal weight evaluation func.
Hue-emphasized evaluation func.
Brightness-emphasized evaluation func.

Fig. 9(a)

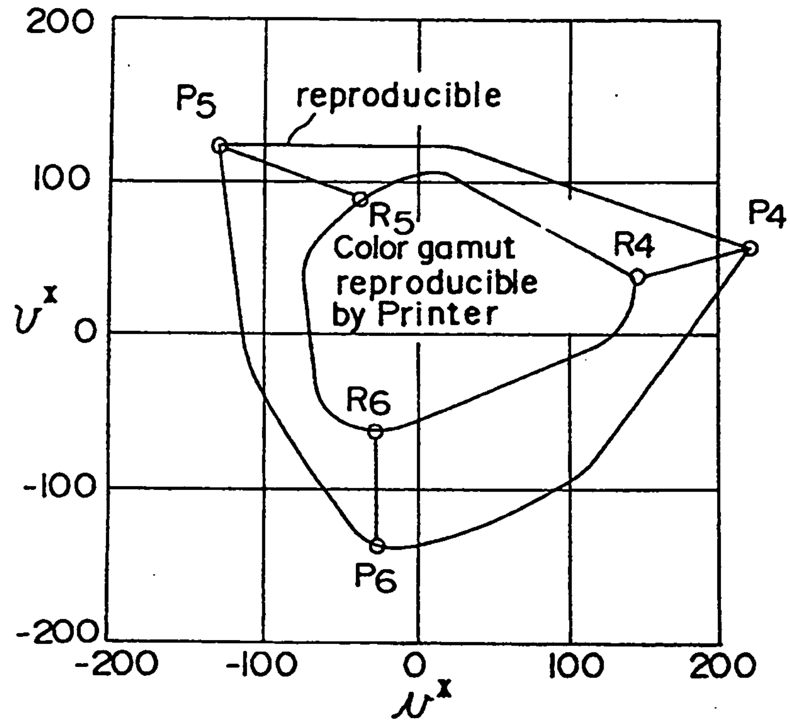


Fig. 9(b)

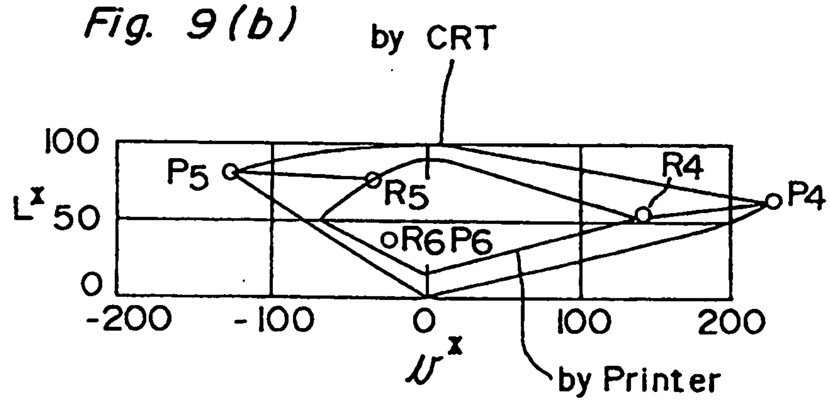


Fig. 9(c)

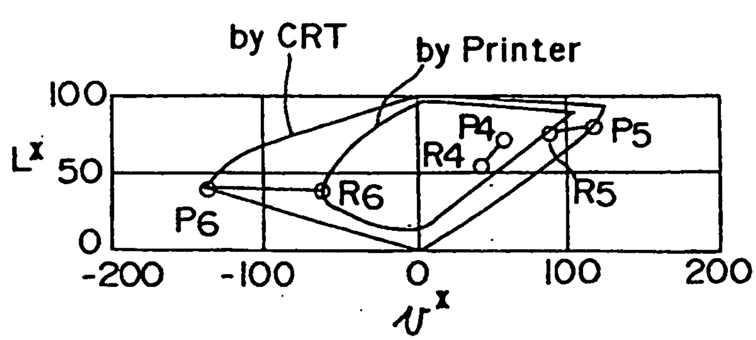


Fig. 10

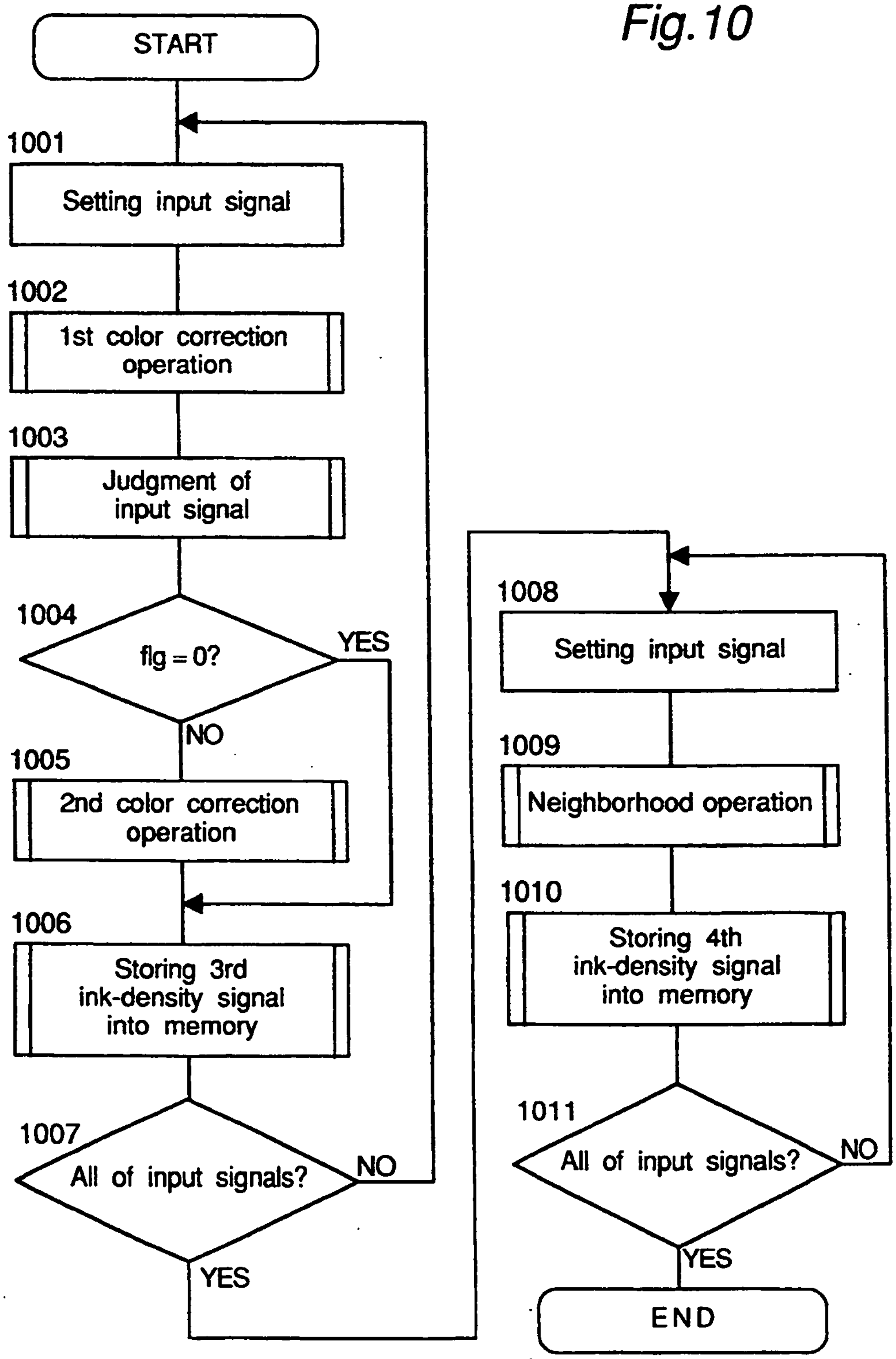

START
1001
Setting input signal
1002
1st color correction operation
1003
Judgment of input signal
1004
flg = 0?
YES
NO
1005
2nd color correction operation
1006
Storing 3rd ink-density signal into memory
1007
All of input signals?
NO
YES
1008
Setting input signal
1009
Neighborhood operation
1010
Storing 4th ink-density signal into memory
1011
All of input signals?
NO
YES
END

Fig. 11 (a)

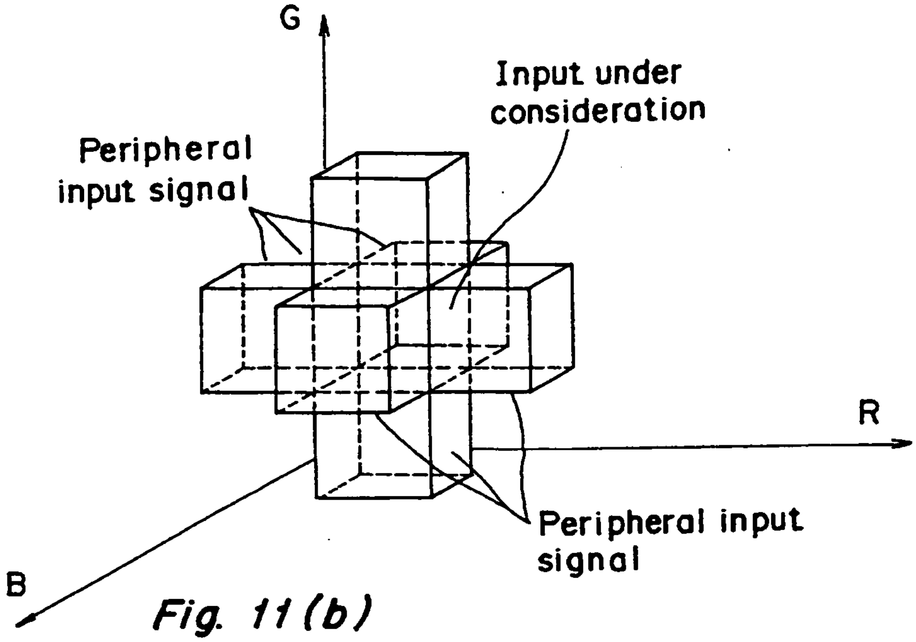


Fig. 11 (b)

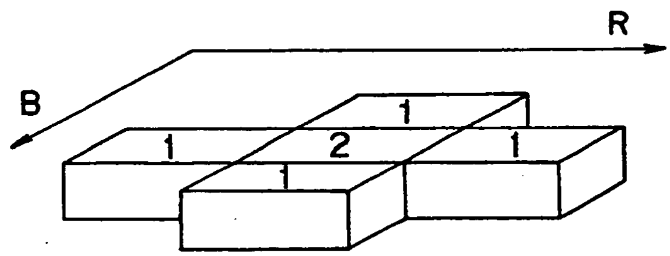


Fig. 11 (c)

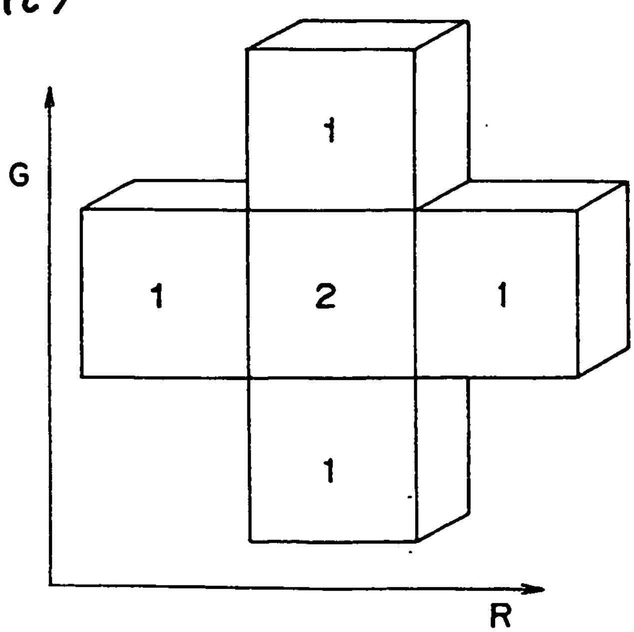


Fig. 12(a)

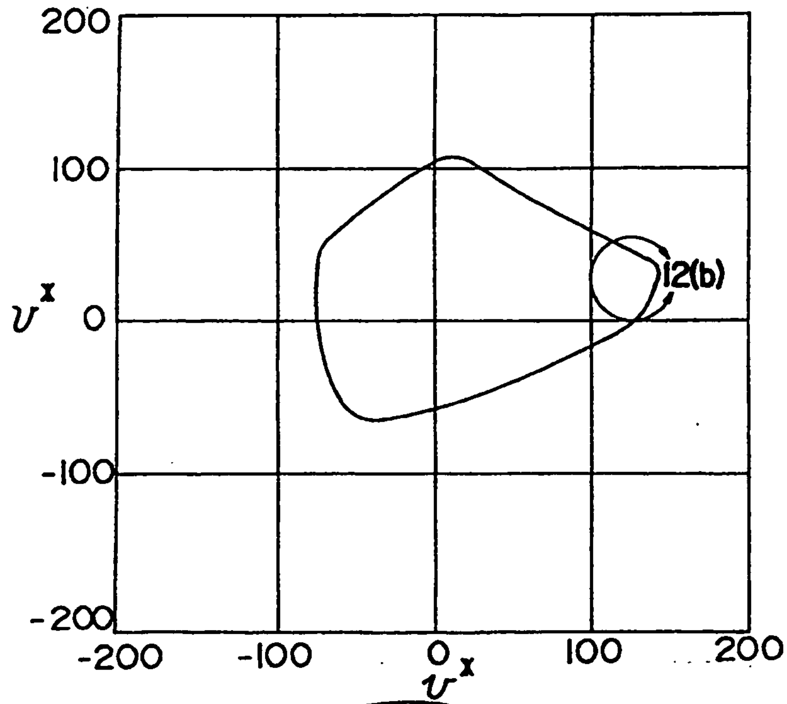
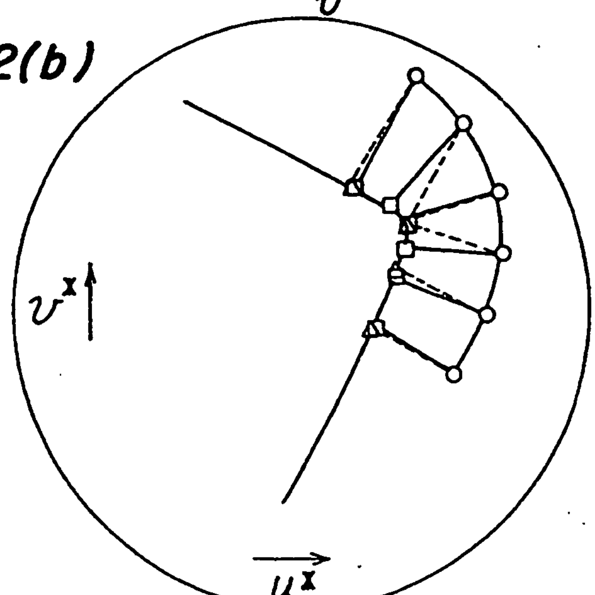
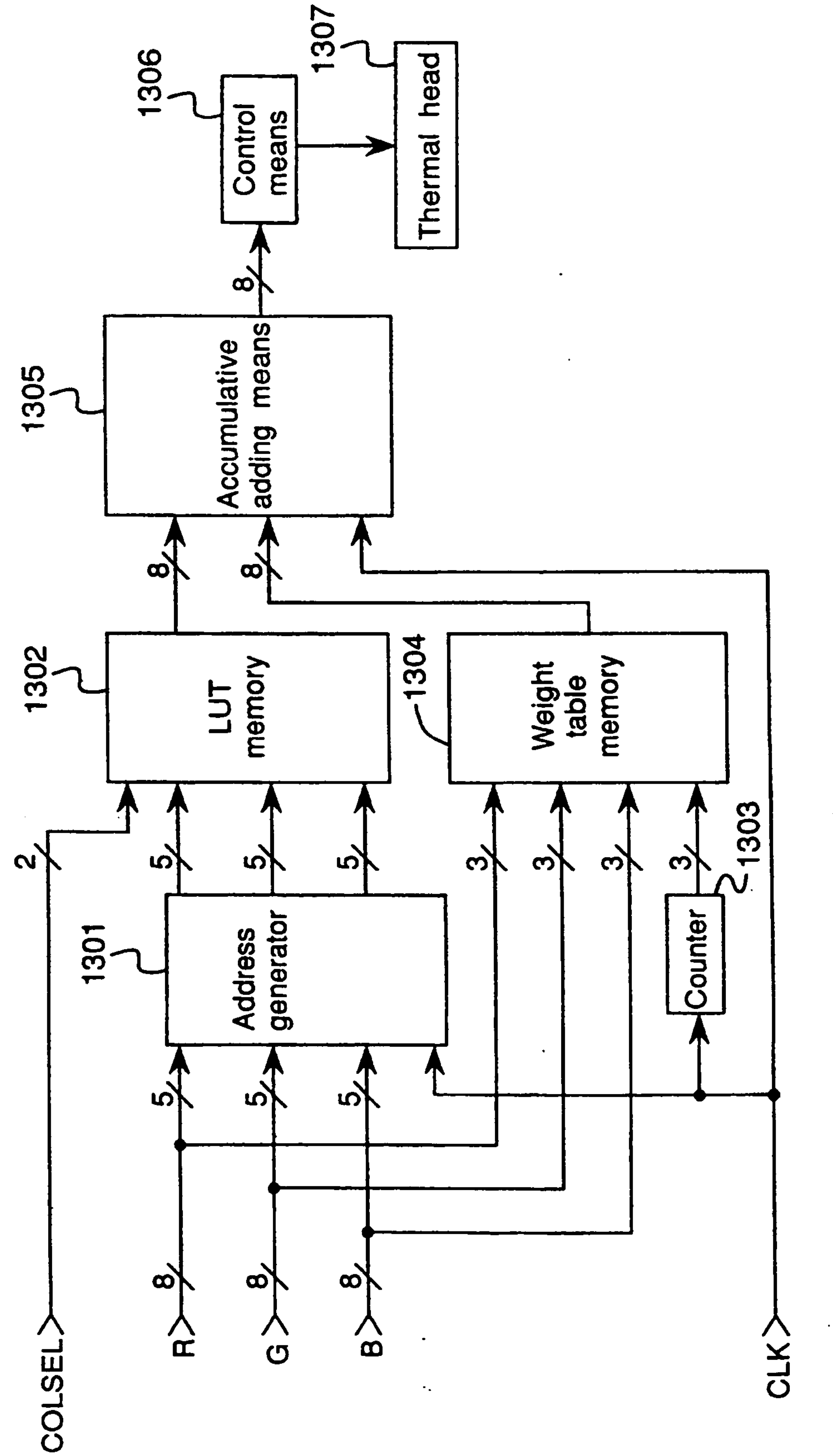


Fig. 12(b)





1306
Control means
1307
Thermal head
8
1305
Accumulative adding means
8
8
1302
LUT memory
1304
Weight table memory
2
5
5
5
3
3
3
3
1303
1301
Address generator
Counter
5
5
5
8
8
8
COLSEL
R
G
B
CLK

Fig. 13

Fig. 14

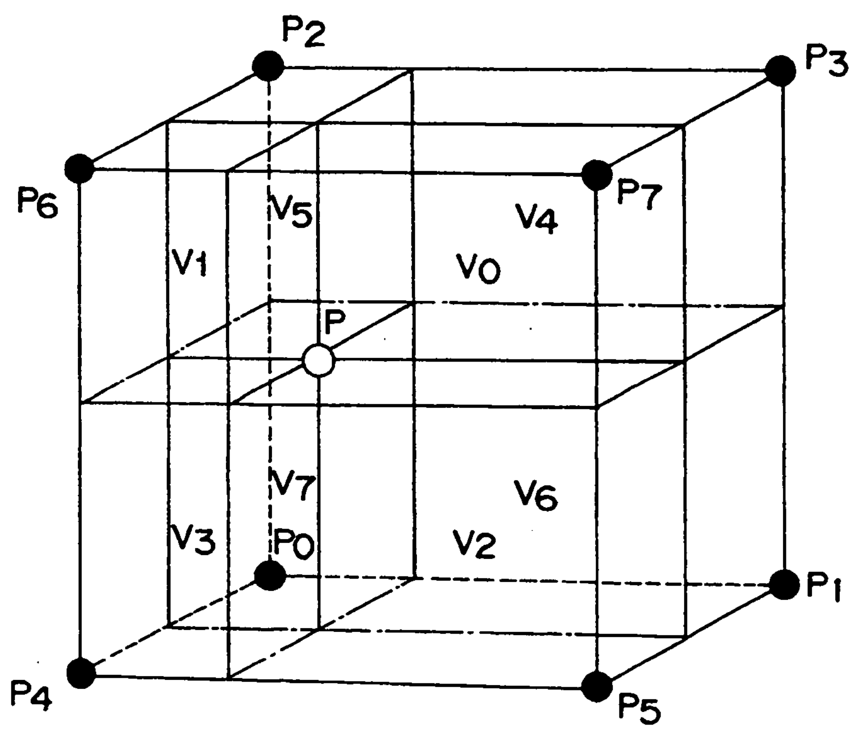


Fig. 15 (a)

Fig. 15 (b)

Fig. 15 (c)

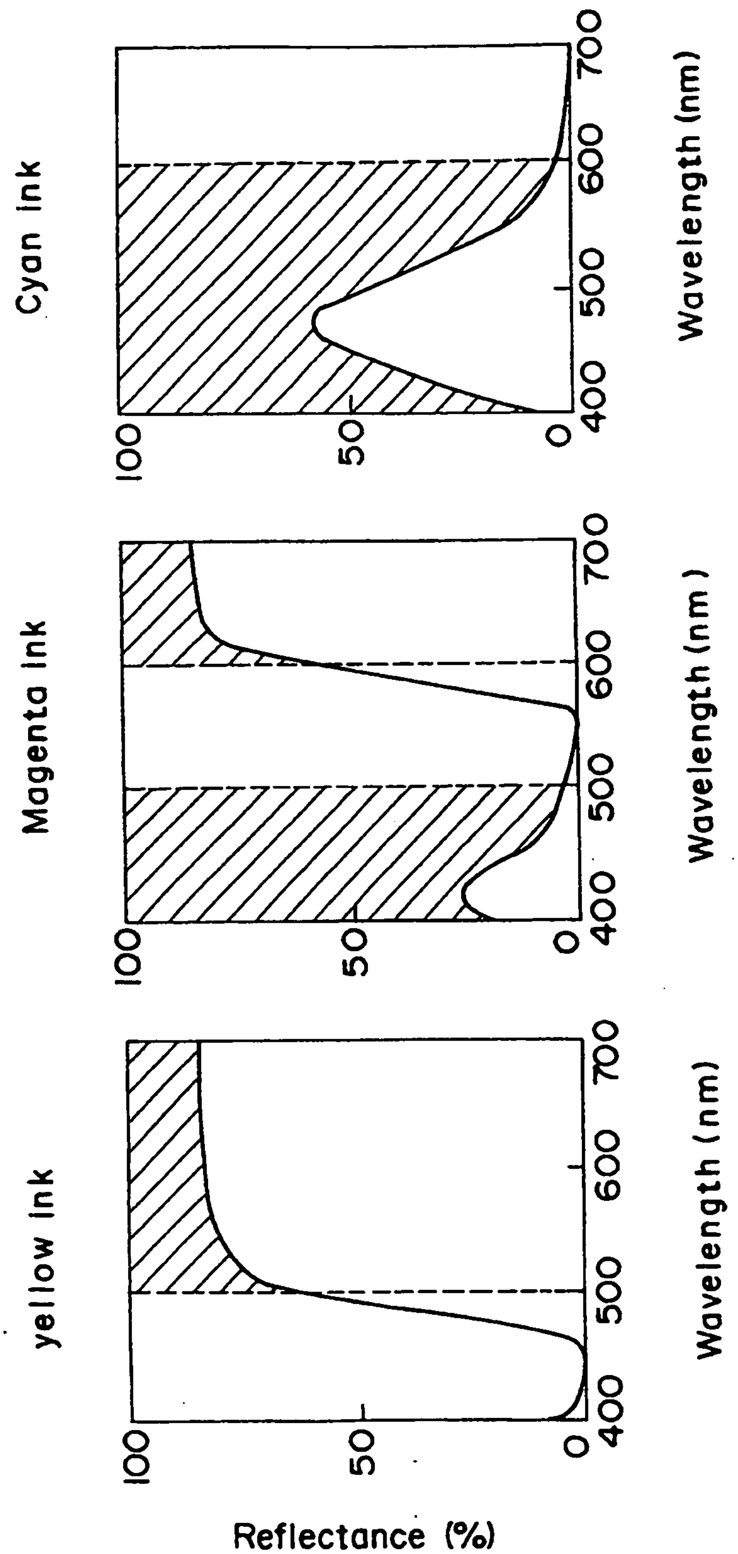


Fig. 16 (a)

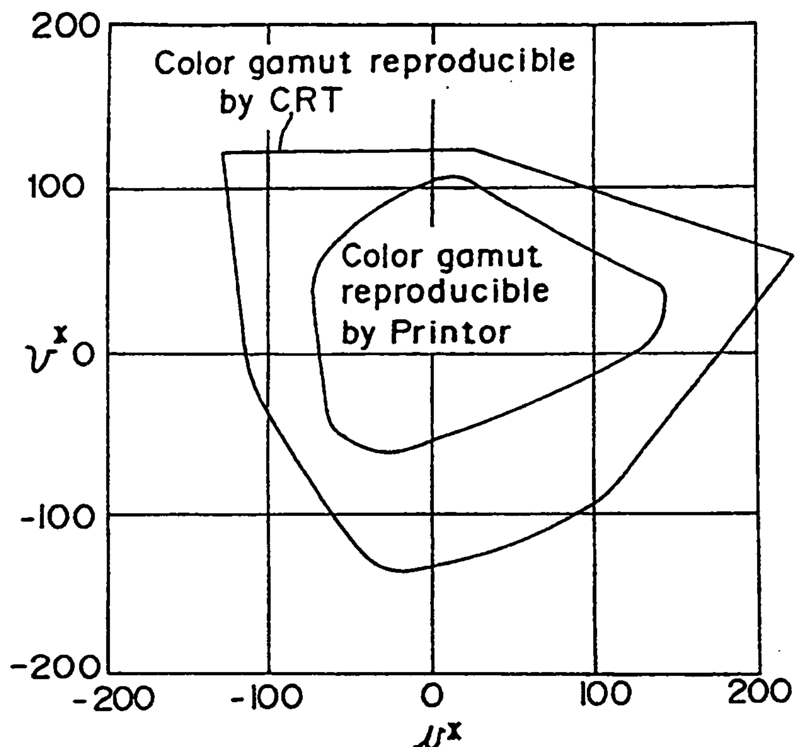


Fig. 16 (b)

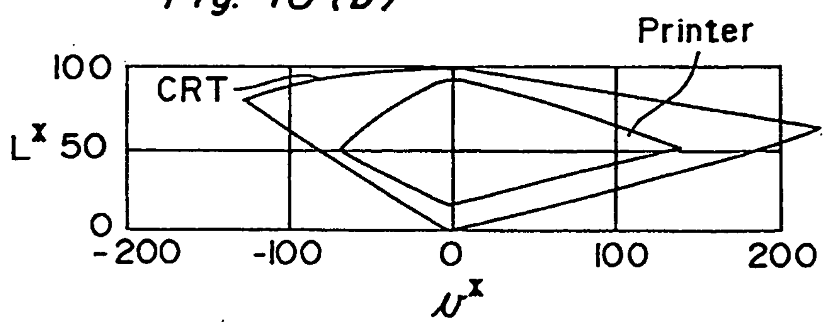


Fig. 16 (c)

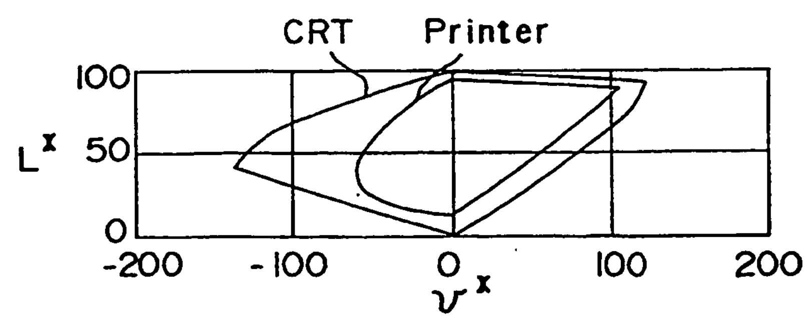


Fig. 17 (a)

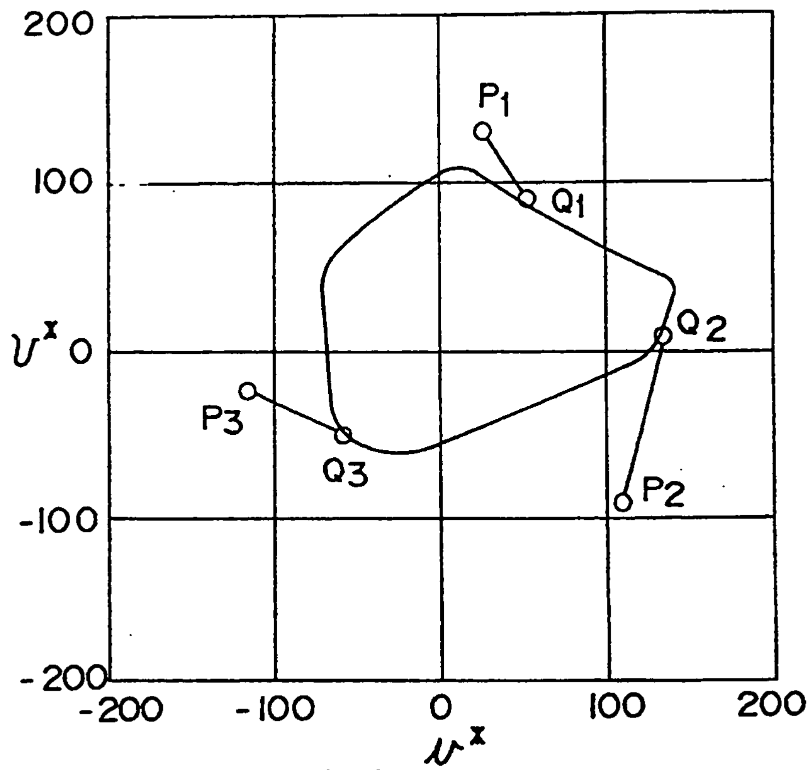


Fig. 17 (b)

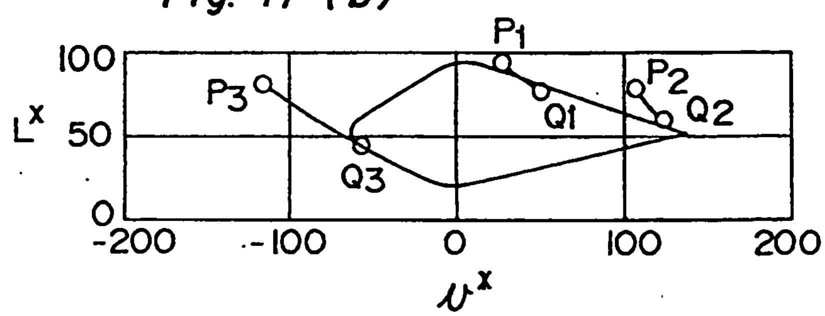
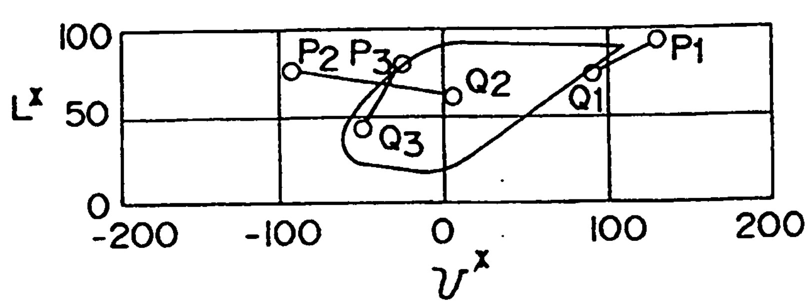


Fig. 17 (c)



METHOD AND APPARATUS FOR FORMING COLOR IMAGES BY CONVERTING A COLOR SIGNAL TO A FURTHER COLOR DENSITY SIGNAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to method and apparatus for forming color images on paper with color inks by color printer, color copy machine or the like.

2. Description of the Related Art

In color CRTs (cathode ray tubes), which are widely used for color television sets, computer monitors and the like, color reproduction is made by controlling the luminances of the primary colors of colored light, red (R), green (G), and blue (B), based on the principle of additive color mixture. On the other hand, color reproduction in hard copying such as by color printer or color copy machine is made by controlling reflectances of colored lights with color inks of cyan (C), magenta (M), and yellow (Y), which are complementary colors of the primaries of colored light, based on the principle of subtractive color mixture.

However, the spectral absorption characteristic of a color ink is broad, as shown in FIGS. 15(*a*), 15(*b*) and 15(*c*) which show the spectral absorption characteristics of inks used in a sublimation type thermal transfer printer, and each ink absorbs unnecessary components other than the complementary colors of its reflected light, so that it does not function as an ideal absorption filter. Therefore, processing called color correction is performed to reproduce desired colors.

A method called masking has been employed for color correction in hard copying. Among the masking methods, most often used is a method called linear masking, which determines an ink-density signal (Y, M, C) by applying a linear operation to a primary color density signal (D_R, D_G, D_B), which expresses the densities of complementary colors of a primary color signal (R, G, B), as shown in the following (1).

$$\begin{bmatrix} C \\ M \\ Y \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} D_R \\ D_G \\ D_B \end{bmatrix} \tag{1}$$

The linear masking assumes that the additive law of densities (Lambert-Beer law) holds in color reproduction that uses real inks and that color reproduction is realized by a linear operation in a whole color space. However, it is known that in color reproduction that uses real inks, eg. by a sublimation type thermal transfer printer, the additive and proportional laws do not hold owing to various nonlinear factors such as resublimation of inks and internal reflection of inks.

Therefore, there has been proposed a nonlinear masking method that determines the density signal (Y, M, C) of inks by a high-degree polynomial. Following is the formula for quadratic masking, which is the simplest nonlinear masking.

$$C = a_0 D_R + a_1 D_g + a_2 D_B + a_3 D_R^2 + a_4 D_G^2 + a_5 D_B^2 + a_6 D_R D_G + a_7 D_G D_B + a_8 D_B D_R \tag{2}$$

$$M = a_9 D_R + a_{10} D_g + a_{11} D_B + a_{12} D_R^2 + a_{13} D_G^2 + a_{14} D_B^2 + a_{15} D_R D_G + a_{16} D_G D_B + a_{17} D_B D_R$$

-continued

$$M = a_{18} D_R + a_{19} D_g + a_{20} D_B + a_{21} D_R^2 + a_{22} D_G^2 + a_{23} D_B^2 + a_{24} D_R D_G + a_{25} D_G D_B + a_{26} D_B D_R$$

The quadratic masking performs color correction by the quadratic equations incorporating nonlinear factors in color reproduction, and the 27 correction coefficients a_0 to a_{26} are determined by the least square method with respect to differences of color densities. (See for example, Image processing for color reproduction, Imaging Part 1, Shashin Kogyo Bessatsu).

Further, color reproduction for hard copying has a problem of the reproducible color gamut. The range of densities realized by a color printer is limited to the maximum printing density inherent to each printer and the density of the paper used for reproduction. Owing to this limitation on the printable densities and the existence of unnecessarily absorbed components, the range of reproducible colors is limited, so that the color gamut reproducible by a color printer is generally smaller than that by a CRT, which employs the principle of additive color mixture.

FIG. 16 shows the color gamuts reproducible by a CRT and a color printer in the perceptually uniform CIE L*u*v* color space. FIG. 16 (*a*) shows the projection of the color reproduction gamuts on the u*v* plane, FIG. 16 (*b*) shows the projection on the L*u* plane, and FIG. 16 (*c*) shows the projection on the L*v* plane In FIG. 16, the color reproduction range of a printer is of the printer whose spectral absorption characteristics are shown in FIG. 15, and the color reproduction gamut of a CRT is of a CRT in the NTSC system.

Since the color reproduction gamut of a printer is smaller than that of a CRT in this way, a signal that requests a color outside the color reproduction gamut of a printer is sometimes input to the printer. This case happens when at least one of the density values (Y, M, C) determined by linear masking or nonlinear masking described above is less than the density of the paper or greater than the maximum density of the printer. Prior arts have performed printing for this unreproduceable ink density using limiters that set the density value to the density of the paper if a density less than the density of the paper is requested and sets the value to the density of the maximum density of the printer if a density greater than the maximum density of the printer is requested.

However, since a density signal of inks and colors people perceive are in nonlinear relations, the limiters for an ink-density signal do not provide optimal adjustment. FIG. 17 shows examples of color reproduction when limiters are used for an ink-density signal obtained by a masking operation. In FIG. 17, P_i, i=1, 2, 3, are desired colors indicated by input signals, and Q_i, i=1, 2, 3, are the corresponding colors indicated by the limiters.

Alternatively, there has been proposed a color correction circuit comprising means for performing a primary correction operation for correcting an output signal (ink density signals) to have a proportional relationship with an input signal (primary color density signals), means for performing a secondary correction operation for minimizing a difference between the density of an input image and that of an output image using the least square method and means for selecting the result obtained by the secondary correction operation if

a difference between the result and the input signal is smaller than a predetermined value and, if not, the result obtained by the primary correction operation (See JP-A SHO 63-151263).

Also, there has been proposed a color image processing apparatus in which there is provided a look-up table storing data for judging whether or not an input signal is within the color gamut reproducible by the output apparatus and, if judged that the input signal is within the color gamut, by referring to the look-up table, outputs from a density conversion table are selected and, if judged that it is out of the color gamut, outputs from logarithmic conversion circuit and masking circuit (See JP-A HEI 4-181870).

Thus, according to these prior arts, the ink density signals are determined by a masking operation when the input signal is out of the color gamut reproducible by a printer.

However, since the color gamut of the input signal is wider than that reproducible by a printer, results obtained by masking operation to the input signal out of the color reproduction gamut of the printer contains ink density signals impossible to reproduce by the printer and, therefore, necessitating to subject them to limiting operation.

It is considerable to set correction coefficients for the masking operation so that the ink density signals reproducible by the printer may be obtained even to the input signal out of the color gamut reproducible by the printer. However, in this method, a very large compression of a color space is performed by the masking operation and, therefore, color reproduction may be made using colors very different from input colors resulting in an unnatural color reproduction.

As shown in the above examples, when desired colors corresponding to an input color signal are outside the color gamut reproducible by a printer, prior arts sometimes perform color reproduction using greatly different colors from the ones that people feel to be better, even the better colors exist within the color gamut reproducible by the printer.

SUMMARY OF THE INVENTION

The object of the present invention is therefore to provide a method and apparatus of forming color images of which people do not feel the degradation of image quality by performing color reproduction using optimal colors within the range of colors reproducible by a printer, if a color signal that can not be realized by the printer is given.

In order to achieve the aforementioned objective, the method of forming color images in accordance with the present invention comprises a first color correction process that performs optimal color correction for colors reproducible by a printer and converts an input color signal into a first color density signal (Y1, M1, C1), a judgment process that judges whether the input signal indicate a color reproducible by the printer, a second color correction process that converts the input signal judged to indicate a color unreproduceable by the printer in the judgment process into a second color density signal (Y2, M2, C2) that produce an optimal color within the range of colors reproducible by the printer. The method then controls ink densities and forms color images following the judgment process, using the first color density signal (Y1, M1, C1) if the input signal indicates a color reproducible by the printer, and using the second color density signal (Y2, M2, C2) if the input signal indicates a color unreproduceable by the printer.

It is to be noted that the term "color density signal" indicates a signal for controlling densities of yellow, magenta and cyan materials used in a color image forming apparatus. Namely, it indicates an color density signal in the case that yellow, magenta and cyan inks are used and, in the case that yellow, magenta and cyan toners are used, it indicates a toner-density signal.

Further, in order to achieve the aforementioned objective, the apparatus of forming color images in accordance with the present invention converts a representative point indicated by upper bits of each input signal into a first color density signal (Y1, M1, C1) by a first color correction operation that performs optimal color correction for colors reproducible by the printer, judges whether the representative point indicates a color reproducible by the printer, converts the representative point that indicates a color unreproduceable by the printer into a second color density signal (Y2, M2, C2) by a second color correction operation, and following the above judgment, determines the color density signal (Y3, M3, C3) of the above representative point to be the first color density signal (Y1, M1, C1) if the input signal indicates a color reproducible by the printer and determines the color density signals (Y3, M3, C3) of the above representative point to be the second color density signal (Y2, M2, C2) if the input signal indicates a color unreproduceable by the printer. The apparatus has a memory means composed of a ROM or RAM that stores the above color density signal (Y3, M3, C3), an address means that receives upper bits of the input signal to be printed and generates an address to be given to the above memory means, and an interpolation means that performs an interpolation operation using the color density signal (Y3, M3, C3) output from the above memory means and lower bits of the input signals to be printed and determines the color density signal (Y, M, C) corresponding to the input signal to be printed. Finally, the apparatus performs color printing using the color density signal (Y, M, C).

The method of forming color images in accordance with the present invention performs color reproduction using an optimal color for even an input signal that indicates a color unreproduceable by a printer, so that the method greatly improves image quality. This effect is due to the fact that the method uses the first color density signal for an input signal that indicates a color reproducible by a printer and uses the second color density signal for an input signal that indicates a color unreproduceable by a printer.

Further, the apparatus of forming color images in accordance with the present invention performs the determination of the color density signal by real-time processing even for an input signal that indicates a color unreproduceable by a printer. The apparatus performs color printing of a full color image having high image quality for input signals that indicate colors including those unreproduceable by a printer.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects and features of the present invention will become clear from the following description taken in conjunction with the preferred embodiments thereof with reference to the accompanying drawings throughout which like parts are indicated by like reference numerals, and in which:

FIG. 1 shows a flowchart of the method of forming color images in the first embodiment in accordance with the present invention;

FIG. 2 shows a block diagram of an image forming apparatus used in the first embodiment;

FIG. 3 shows a detailed flowchart of the judgment process in the first embodiment; FIG. 4(*a*) shows a schematic color gamut reproducible by a printer in the ink-density space and FIGS. 4(*b*), 4(*c*) and 4(*d*) are projections of the color gamut on Y–C, C–M, and M–Y planes, respectively;

FIG. 5 shows a detailed flowchart of the second color correction process in the first embodiment;

FIGS. 6(*a*), 6(*b*) and 6(*c*) show a result of a color reproduction by the first embodiment with respect to μ^*-v^*, μ^*-L^* and v^*-L^* planes of a perceptually-uniform color space, respectively;

FIG. 7 shows a detailed flowchart of the second color correction process in the method of forming color images in the second embodiment in accordance with the present invention;

FIGS. 8(*a*) and 8(*b*) show examples of an evaluation function in the second color correction operation of the second embodiment, respectively;

FIGS. 9(*a*), 9(*b*) and 9(*c*) are projections onto μ^*-v^*, μ^*-L^* and v^*-L^* planes for showing a result of an experimental color reproduction by the second embodiment in a perceptually-uniform color space, respectively;

FIG. 10 shows a flowchart of the processing that creates a table of ink-density signals for input signals in the method of forming color images in the third embodiment in accordance with the present invention;

FIG. 11(*a*) shows input signals used for a typical neighborhood operation in the third embodiment, and FIGS. 11(*b*) and 11(*c*) are those when seen in B–R and R–G planes, respectively;

FIGS. 12(*a*) and 12(*b*) show an experimental result of color reproduction by the third embodiment in a perceptually-uniform color space;

FIG. 13 shows a block diagram of the apparatus of forming color images in the fourth embodiment;

FIG. 14 shows a method of interpolation by the apparatus of forming color images in the fourth embodiment;

FIGS. 15(*a*), 15(*b*) and 15(*c*) show the spectral absorption characteristics of inks used in a sublimation type thermal transfer printer, respectively;

FIGS. 16(*a*), 16(*b*) and 16(*c*) show color gamuts reproducible by a CRT and a printer with respect to μ^*-v^*, μ^*-L^* and v^*-L^* planes, respectively;

FIGS. 17(*a*), 17(*b*) and 17(*c*) show color reproduction by a prior method of forming color images with respect to μ^*-v^*, μ^*-L^* and v^*-L^* planes, in case an input signal indicates a color unreproduceable by a printer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments according to the present invention will be described below with reference to the attached drawings.

In the following is described the method of forming color images in the first embodiment in accordance with the present invention. The first embodiment determines an ink-density signal (Y, M, C) by software for printing or reproducing color images by a printer based on a primary color luminance signal (R, G, B) that is used for a CRT. The first embodiment employs a sublimation type thermal transfer full-color printer using three color inks of yellow, magenta, and cyan.

A block diagram of an apparatus used in the first embodiment is shown in FIG. 2. In FIG. 2, reference numeral 201 denotes a CPU that performs the method forming color images in accordance with the present invention. 202 denotes a RAM that is used for a work area for CPU 201 in executing a program. 203 denotes a ROM that is used as storage for the program executed by CPU 201. 204 denotes an I/O means that reads input signals (R, G, B) to be printed and outputs ink-density signals (Y, M, C). 205 denotes a bus that connects each of CPU 201, RAM 202, ROM 203, and I/O means 204 with each other. 206 denotes a controller that controls impression energy based on the ink-density signal (Y, M, C) output from I/O means 204. 207 denotes a thermal head that impresses an ink sheet, which is not shown in FIG. 2, with the impression energy controlled by controller 206 and forms a full color image on an image-receiving sheet of paper, which is not shown in FIG. 2.

The first embodiment realizes the method of forming color images in accordance with the present invention in the apparatus composed as above by software. A flowchart of overall processing performed by CPU 201 is shown in FIG. 1, and detailed flowcharts of subroutines of the main processing are shown in FIGS. 3 and 5.

First, overall procedure is described referring to FIG. 1.

Step 101 inputs an input signal (R, G, B) to be printed through I/O means 204.

Step 102 is a first color correction process, which performs optimal color correction for a color reproducible by a printer for an input signal (R, G, B) and obtains a first ink-density signals (Y1, M1, C1).

Step 103 is a judgment process, which judges whether the input signal (R, G, B) indicates a color reproducible by the printer based on the first ink-density signals (Y1, M1, C1). If the input signal indicates a color reproducible by the printer, then Step 103 sets a flag signal flg as flg=0. If not, then Step 103 sets flg=1.

Step 104 is a conditional branch instruction. If flg=0, i.e. the input signal (R, G, B) indicates a color reproducible by the printer, then the processing proceeds to Step 106. If flg=1, i.e. the input signal (R, G, B) indicates a color unreproduceable by the printer, then the processing proceeds to Step 105.

Step 105 is a second color correction process, which performs a second color correction operation for an input signal which can not be realized by the printer and obtains a second ink-density signal (Y2, M2, C2) that produces an optimal color reproducible by the printer.

Step 106 outputs an ink-density signal (Y, M, C) from I/O means 204 depending on the flag signal flg. If flg=0, then (Y, M, C)=(Y1, M1, C1), and if flg=1, then (Y, M, C)=(Y2, M2, C2).

Then controller 206 controls the heat quantities of thermal head 207 in the face order of yellow, magenta, and cyan depending on the ink-density signal (Y, M, C) output from I/O means 204, so that gradation reproduction is performed on an image-receiving sheet of paper and a color image is formed.

Next, the first color correction process performed by Step 102 is described in the following. In "the present embodiment, a mixed operation composed of linear operation for luminance signals and nonlinear masking

operation for density signals is used for the first color correction. The details are as follows.

First, the following luminance matrix operation (3) is applied to the input signal (R, G, B) to obtain a second luminance signal (R′, G′, B′) in order to correct the difference of the central wavelengths between the spectral characteristics of the phosphor used in the CRT and the spectral absorption characteristics of the inks used in the printer.

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} \tag{3}$$

Next, each component of the second luminance signal (R′, G′, B′) is converted into a component of a primary color density signal (D_R, D_G, D_B) for subtractive mixture of colors by the following complementary color transformation (4).

$$D_R = \log_{10}(1/R')$$

$$D_G = \log_{10}(1/G')$$

$$D_B = \log_{10}(1/B') \tag{4}$$

Further a nonlinear masking operation is applied to correct color turbidity caused by components of light unnecessarily absorbed by inks.

First, the primary color density signal is converted into a signal corresponding to color materials of inks. Specifically, if a constant that expresses the degree of nonlinearity in the relation between the color materials of inks and the color densities is denoted by a, where a >1, then, by a first nonlinear transformation formula shown in the following (5), the primary color density signal (D_R, D_G, D_B) is converted into a signal (C′, M′, Y′) corresponding to color materials of inks.

$$C' = D_R^{a}$$

$$M' = D_G^{a}$$

$$Y' = D_B^{a} \tag{5}$$

Next, by a linear transformation shown in the following (6), the output signal (C′, M′, Y′) of the first nonlinear transformation is converted into (C″, M″, Y″).

$$\begin{bmatrix} C'' \\ M'' \\ Y'' \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} C' \\ M' \\ Y' \end{bmatrix}. \tag{6}$$

Further, (C″, M″, Y″) is converted into (Y1, M1, C1) by the following (7), which is the inverse of (5).

$$C1 = C''^{1/a}$$

$$M1 = M''^{1/a}$$

$$Y1 = Y''^{1/a} \tag{7}$$

In the present embodiment, the correction coefficients $\{b_{kl}\}$ of (3), $\{a_{kl}\}$ of (6), where, k=1, 2, 3, and l=1, 2, 3, and the constant a of (5) and (7) are determined by a successive approximation so that the average errors between each color reproduced by a CRT and the corresponding color reproduced by the printer for about color chips uniformly located in the color gamut reproducible by the printer. The actual values of these correction coefficients are as follows.

$$\begin{bmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \end{bmatrix} = \begin{bmatrix} 0.896 & 0.096 & 0.008 \\ 0.002 & 0.835 & 0.163 \\ 0.068 & -0.035 & 0.967 \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} = \begin{bmatrix} 1.443 & -0.105 & 0.037 \\ -0.360 & 1.694 & -0.032 \\ 0.002 & -0.679 & 1.978 \end{bmatrix}$$

$$a = 1.572$$

The first color correction operation used in the present embodiment performs color correction for colors reproducible by the printer with the color difference Euv=4.3 on an average in the perceptually-uniform color space.

Next, the judgment process (Step **103**) that judges whether or not an input signal (R, G, B) indicates a color reproducible by the printer is described in detail in the following.

FIG. **4** shows the color gamut reproducible by the printer in the ink-density space, which expresses the density of each ink of yellow (Y), magenta (M), and cyan (C) by a coordinate on the corresponding axis. FIG. **4** (*a*) shows a perspective view of the color gamut. FIG. **4** (*b*) shows the color range projected on the YC plane. FIG. **4** (*c*) shows the color range projected on the MC plane. FIG. **4** (*d*) shows the color range projected on the YM plane. As shown in FIGS. **4**(*a*) to **4**(*d*), the color gamut is determined by the density that can be reproduced by each ink. If the color densities of the paper used for printing of yellow, magenta, and cyan are respectively denoted by Y0, M0, C0, and the corresponding maximum densities that can be printed are respectively denoted by Ymax, Mmax, Cmax, then the color range is the rectangular solid enclosed by the six planes, Y=Y0, M=M0, C=C0, Y=Ymax, M=Mmax, C=Cmax.

Therefore, when a first color correction operation performs optimal color correction for colors reproducible by the printer, whether the input signal (R, G, B) indicates a color reproducible by the printer is judged by testing whether Y0≦Y1≦Ymax, M0≦M1≦Mmax, and C0≦C1≦Cmax for the first ink-density signal (Y1, M1, C1) obtained by the first color correction process. Step **103** performs this test. The detail is described in the following referring to the flowchart of FIG. **3**.

Step **301** tests whether Y0≦Y1≦Ymax or not. If not, then the input signal is judged to indicate a color unreproduceable by the printer. Similarly, step **302** tests whether M0≦M1≦Mmax or not, and Step **303** tests whether C0≦C1≦Cmax or not.

If the input signal is judged to indicate a color unreproduceable by the printer by one of Steps **301**, **302**, and **303**, then Step **305** sets flg=1. If the input signal satisfies all the test conditions of Steps **301**, **302**, and **303**, then Step **304** sets flg=0.

In this way, the present embodiment judges whether the input signal (R, G, B) indicates a color reproducible by the printer based on the first ink-density signal (Y1, M1, C1) obtained by the first color correction process.

Next, the second color correction process (Step 105) is described in the following. The second color correction operation first obtains the color indicated by the input signal (R, G, B), i.e. a target color for color reproduction by the printer. Then the second color correction operation sets ink-density signals, obtains predicted colors realized by the ink-density signals, chooses an optimal ink-density signal such that an evaluation value calculated by the target color and the predicted color becomes minimal. FIG. 5 shows a detailed flowchart of the second color correction process. First, Step 501 converts the input signal (R, G, B) into a color signal of a target color for color reproduction by the printer. In the present invention, the input signal is a primary color luminance signal (R, G, B) that drives a CRT. Therefore, tristimulus values (X_0, Y_0, Z_0), which are reproduced when the primary color luminance signal is input to a CRT of the NTSC system, is obtained by the following output equation (9) for a CRT of the NTSC system.

$$\begin{bmatrix} X_0 \\ Y_0 \\ Z_0 \end{bmatrix} = \begin{bmatrix} 0.60699 & 0.17345 & 0.20057 \\ 0.29897 & 0.58642 & 0.11461 \\ 0.0 & 0.066075 & 1.11586 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} \tag{9}$$

Further, considering human visual characteristics, the tristimulus values (X_0, Y_0, Z_0) are converted into the coordinates (L_0^*, u_0^*, v_0^*) in the perceptually uniform $L^*u^*v^*$ space by the following (10).

$$\begin{aligned} L_0^* &= 116(Y_0/Y_n)^{1/3} - 16, \text{ if } Y_0/Y_n > 0.008856 \\ &= 903.29(Y_0/Y_n), \text{ if } Y_0/Y_n \leq 0.008856 \end{aligned} \tag{10}$$

$$u_0^* = 13L_0^*(u_0' - u_n')$$
$$v_0' = 13L_0^*(v_0' - v_n')$$

where

$$u_0' = 4x_0/(X_0 + 15Y_0 + 3Z_0)$$

$$v_0' = 9Y_0/(X_0 + 15Y_0 + 3Z_0)$$

and

$$Y_n = 100$$

$$u_n' = 0.2009$$

$$v_n' = 0.4609$$

if a standard light source used for illumination is the C light source and the field of view is 2 degrees wide.

Next, Step 502 sets values of an ink-density signal to search for an optimal ink-density signal.

Step 503 predicts the color (L_i^*, u_i^*, v_i^*) reproduced by the printer when the ink-density signal set by Step 502 is used.

Step 504 obtains the evaluation value Euv for the set ink-density signal using the target color (L_0^*, u_0^*, v_0^*) and the predicted color (L_i^*, u_i^*, v_i^*). The evaluation value Euv in the present embodiment is the color difference in the perceptually uniform space between the target color and the predicted color defined by the following (11).

$$Euv = \{(L_0^* - L_i^*)^2 + (u_0^* - u_i^*)^2 + (v_0^* - v_i^*)^2\}^{1/2} \tag{11}$$

Step 505 judges whether the Euv obtained by Step 504 is minimal or not.

Step 506 stores the ink-density signal set by Step 502 as the second ink-density signal (Y2, M2, C2), if Step 505 judges that the Euv is minimal.

Step 507 tests if the search for an optimal ink-density signal has been finished or not. If the search has not been finished, then the processing returns to Step 502, and repeats Steps from 503 to 507.

Next, the prediction of color reproduction in Step 503 for a set ink-density signal is described in the following. The first color correction operation in the present embodiment is a nonlinear operation including the nonlinear transformations (4), (5), and (7). Since each of these nonlinear transformations and linear transformations (3) and (6) is a one-to-one transformation, a conversion of the ink-density signal into a primary color luminance signal can be obtained by the inverse of the first color correction operation. Therefore, the present embodiment performs the prediction of color reproduction by converting the ink-density signal into a primary color luminance signal and then converting the results into the color signal in the perceptually-uniform color space in the same way as a target color is obtained.

Specifically, the set ink-density signal (C2, M2, Y2) is converted into (C2'', M2'', Y2'') by the following nonlinear transformation (12).

$$C2'' = C2^a$$

$$M2'' = M2^a$$

$$Y2'' = Y2^a \tag{12}$$

Then (C2'', M2'', Y2'') is converted into (C2', M2', Y2') by the following (13), which is the inverse of transformation (6).

$$\begin{bmatrix} C2' \\ M2' \\ Y2' \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix}^{-1} \begin{bmatrix} C2'' \\ M2'' \\ Y2'' \end{bmatrix} \tag{13}$$

Then (C2', M2', Y2') is converted into a primary color luminance signal ($D2_R$, $D2_G$, $D2_B$) by the following nonlinear transforation (14).

$$D2_R = C2'^{1/a}$$

$$D2_G = M2'^{1/a}$$

$$D2_B = Y2'^{1/a} \tag{14}$$

Further, ($D2_R$, $D2_G$, $D2_B$) is converted into a luminance signal (R2', G2', B2') of additive color mixture by the inverse of the complementary color transformation (4).

$$R2' = 10^{-D2R}$$

$$G2' = 10^{-D2G}$$

$$B2' = 10^{-D2B} \tag{15}$$

Then (R2', G2', B2') is converted into a primary color luminance signal (R2, G2, B2) by the following linear transformation (16), which is the inverse of (3).

$$\begin{bmatrix} R2 \\ G2 \\ B2 \end{bmatrix} = \begin{bmatrix} b_{11} & b_{12} & b_{13} \\ b_{21} & b_{22} & b_{23} \\ b_{31} & b_{32} & b_{33} \end{bmatrix}^{-1} \begin{bmatrix} R2' \\ G2' \\ B2' \end{bmatrix} \quad (16)$$

Finally, (R2, G2, B2) is converted into tristimulus values (X_i, Y_i, Z_i) by the transformation of (9) and then converted into coordinates (L_i^*, u_i^*, v_i^*) by the transformation of (10).

As mentioned before, the first color correction operation is performed with Euv=4.3 on an average for colors reproducible by the printer. The second color correction operation is also performed with about Euv=4.3.

Results of an experimental color reproduction by the first embodiment are shown in FIG. 6, which plots target colors and corresponding reproduced colors in the perceptually uniform L*u*v* space. In FIG. 6, P_i, i=1, 2, 3, are target colors which are unreproduceable by a printer, Q_i, i=1, 2, 3, are corresponding colors reproduced by a prior techniques using a masking operation and limiters, and R_i, i=1, 2, 3, are colors reproduced by the present embodiment. It is observed that the color correction of the present embodiment uses a color reproducible by the printer and locating apart from its target color by a minimal distance.

In this way, the present embodiment performs color correction using a color reproducible by a printer and having a minimal distance from its target color in the perceptually uniform space to improve image quality.

The composition of the apparatus, the process of determining the ink-density signal for an input signal, and experimental results have been described above for the first embodiment.

In the present embodiment, the judgment on whether an input signal indicates a color reproducible by a printer or not is performed using the result of the first color correction operation. Among methods not using this result, there is a method that uses a table of judgment results on whether each of all possible input signals is reproducible by a printer or not. The table is made, for example, by expressing colors reproducible by a printer as a range of the perceptually-uniform color space, and comparing each input signal with this range. Since the color gamut reproducible by a printer has a complex shape in the space of input color signals, a vast amount of time is necessary to make the table. Moreover, if an input signal is expressed by 8 bits for each color, then a large memory of 2^{24} bits is needed. In contrast, the judgment method of the present embodiment requires the comparison operation for the first ink-density signals (Y1, M1, C1), so that the processing time is saved when the judgment is performed by software, and the circuit scale is saved when the judgment is implemented by hardware.

In the present embodiment, the prediction about color reproduction for a set ink-density signal is made by the inverse operation of the first color correction operation. Among methods of predicting color reproduction for a set ink-density signal is a method of using a table showing the correspondence between ink-density signals and color measurements of color chips made by ink-density signals. The color chips are prepared for colors situated in a boundary of the color range reproducible by the printer, i.e. for each ink-density signal such that at least one of its values is a color density of the used paper or the maximum density of the color.

The prediction for the ink-density signal not listed on the table is obtained by interpolation. However, this method needs a large number of color chips and a vast amount of time for measurement. Moreover, since the color gamut reproducible by a printer has a complex shape in the space of input color signals, errors caused by the interpolation become great. In contrast, the method of predicting color reproduction in the present embodiment does not need time and labor for making the table and obtains about the same precision as the first color correction operation.

Next, the second embodiment of the method of forming color images in accordance with the present invention is described in the following. The experimental apparatus used in the second embodiment and the overall flowchart is the same as in the first embodiment, but the second color correction process is different.

The second color correction process in the second embodiment is described in the following. FIG. 7 shows a flowchart of the second color correction process of the second embodiment. The second color correction operation of the present embodiment varies an evaluation function depending on the input signal (R, G, B) and obtains an ink-density signal such that the evaluation value becomes minimal.

First, Step 701 converts the input signal (R, G, B) into a coordinate (L_0^*, u_0^*, v_0^*) in the perceptually uniform L*u*v* color space.

Step 702 determines the evaluation function depending on the input signal.

Step 703 sets an ink-density signal to search for an optimal ink-density signal.

Step 704 predicts the color (L_i^*, u_i^*, v_i^*) reproduced by the printer if the ink-density signal set by Step 703 is used.

Step 705 obtains the evaluation value for the set ink-density signals using the target color (L_0^*, u_0^*, v_0^*) and the predicted color (L_i^*, u_i^*, v_i^*) based on the evaluation function determined by Step 704.

Step 706 judges whether the evaluation value obtained by Step 705 is minimal or not.

Step 707 stores the ink-density signals set by Step 703 as the second ink-density signal (Y2, M2, C2), if Step 706 judges that the Euv is minimal.

Step 708 tests if the search for an optimal ink-density signal has been finished or not. If the search has not been finished, then the processing returns to Step 502, and repeats Steps from 703 to 708.

The prediction by Step 704 of color reproduction for a set ink-density signal is performed by converting the ink-density signal into a color signal in the L*u*v* color space in the same way as in the first embodiment.

Next, the evaluation function that evaluates the optimality of a color reproduced by a printer in the present embodiment is described in the following.

The evaluation function E is given by the following (17), where ΔL, ΔH, and ΔS respectively express differences of lightnesses, hues, and saturations between the target color (L_0^*, u_0^*, v_0^*) and the predicted reproduction color (L_i^*, u_i^*, v_i^*), and a, b, and c are weights. Here, the saturation and hue are those in the L*u*v* color space, and the difference of hues is multiplied by the average of the saturations of the two colors to equalize the units.

$$E=\{(a\Delta L^2+b\Delta H^2+c\Delta S^2)/(a+b+c)\}^{\frac{1}{2}} \quad (17)$$

where

$$\Delta L = L_0^* - L_i^*$$

$$\Delta S = S_0 - S_i$$
$$S_0 = (u_0^{*2} + v_0^{*2})^{\frac{1}{2}}$$
$$S_i = (u_i^{*2} + v_i^{*2})^{\frac{1}{2}}$$

$$\Delta H = |\theta_0 - \theta_i| \cdot (S_i + S_0)/2$$
$$\theta_0 = \tan^{-1}(v_0^*/u_0^*)$$
$$\theta_i = \tan^{-1}(v_i^*/u_i^*)$$

The weights a, b, and c are varied depending on input signals and determined by the target color indicated by the input signals through an experiment of subjective evaluation.

First, the weights of the evaluation function E are determined for 26 input signals that indicate colors located on the boundary of the range of colors reproducible by a CRT in the color space of RGB luminance signals. The target color of each of the 26 signals is obtained by converting the signal into coordinates in the L*u*v* color space. Then three evaluation functions, each having a combination of weights, are used to make three color chips for each of 26 input signals such that the ink-density signal used for making each color chip minimizes each evaluation function. Then each color chip is compared with the corresponding target color, and one color chip is chosen as an optimal color chip by subjective judgment, so that the evaluation function for each of the 26 input signals is determined to be the evaluation function that was used to make the optimal color chip. The three evaluation functions consist of a lightness-emphasized function, where weight a is set greater than b and c, a hue-emphasized function, where weight b is set greater than a and c, and a uniform function, where weights a, b, and c are set equal.

FIG. 8 shows the evaluation functions determined by the above procedure in the RGB luminance color space. FIG. 8(*a*) shows the cube of colors reproducible by a CRT viewed from white (W), and FIG. 8(*b*) shows the cube viewed from black (Bk). Each small circle indicate the coordinate of one of the 26 input signal and its evaluation function. For example, if the target color is blue (B) of the CRT, then the uniform function is its evaluation function. if the target color is green (G) of the CRT, then the lightness-emphasized function is its evaluation function. If the target color is black (Bk) or white (W), then any one of the three evaluation functions can be used.

As shown in FIG. 8, the present embodiment determines the ink-density signal for each input signal using an evaluation function whose weights are continuously varied with input signals.

FIG. 9 shows experimental results of color reproduction by the method of the second embodiment. In FIG. 9, the target colors of the input signals indicating red, green, and blue, which are not reproducible by a printer and their reproduced colors are shown in the L*u*v* space. In FIG. 9, points P4 and R4 respectively show the target color and the reproduced color of red; P5 and R5 respectively show the target color and the reproduced color of green; P6 and R6 respectively show the target color and the reproduced color of blue. Since a hue-emphasized evaluation function is used for the input signal indicating red, red is reproduced as a color having almost the same hue as itself and reproducible by a printer. Similarly, green is reproduced as a color having almost the same lightness, and blue is reproduced as a color having a minimal distance from itself in the perceptually uniform space. White is reproduced as a color having the density of paper, and black is reproduced as a color having the maximal density.

The process of determining the ink-density signal for an input signal, the method of determining the evaluation function depending on input signals, and results of experiments have been described above for the second embodiment.

In this way, the present embodiment performs color correction using colors that are reproducible by a printer and people feel to be most preferable based on evaluation functions depending on input signals, so that image quality is greatly improved.

The present embodiment uses evaluation functions shown in FIG. 8, but since the color gamut reproducible by a printer varies with the printing method of the printer and the spectral characteristics of the inks to be used, evaluation functions vary with printers. Therefore, the evaluation functions of the present invention are not limited to the ones shown in FIG. 8.

Next, the method of forming color images of the third embodiment in accordance with the present invention is described in the following.

The apparatus used in the third embodiment is the same as the one in the first embodiment, but the process of determining the ink-density signals is different. In the third embodiment, the ink-density signals for input signals are stored in RAM 202 as an LUT (look-up table), and the ink-density signal used for each input signal is output by referring to the LUT. The ink-density signals in the LUT are determined using a neighborhood operation in the color space of input signals.

FIG. 10 shows the procedure of determining ink-density signals for the LUT.

First, Step 1001 sets an input signal (R, G, B).

Step 1002 obtains the first ink-density signal (Y1, M1, C1) as in the first embodiment.

Step 1003 judges whether the input signal (R, G, B) indicates a color reproducible by the printer based on the first ink-density signal (Y1, M1, C1). If the input signal indicates a color reproducible by the printer, then Step 1003 sets a flag signal flg as flg=0. If not, then Step 1003 sets flg=1.

Step 1004 is a conditional branch instruction. If flg=0, i.e. the input signal (R, G, B) indicates a color reproducible by the printer, then the processing proceeds to Step 1006. If flg=1, i.e. the input signal (R, G, B) indicates a color unreproduceable by the printer, then the processing proceeds to Step 1005.

Step 1005 obtains, for an input signal (R, G, B) unreproduceable by the printer, the second ink-density signal (Y2, M2, C2) that produces an optimal color reproducible by the printer. The process is the same as of the second color correction process in the first embodiment.

Step 1006 chooses a third ink-density signal (Y3, M3, C3) from the first ink-density signal (Y1, M1, C1) and the second density signal (Y2, M2, C2) depending on the flag signal flg and temporarily stores (Y3, M3, C3) in RAM 202. If flg=0, then (Y3, M3, C3)=(Y1, M1, C1), and if flg=1, then (Y3, M3, C3)=(Y2, M2, C2).

Step 1007 tests if the third ink-density signals (Y3, M3, C3) have been obtained for all input signals. If not, then the procedure returns to 1001; else the procedure proceeds to Step 1008.

From Step 1008 and onward the procedure performs a neighborhood operation for each third ink-density signal (Y3, M3, C3).

Step 1008 sets an input signal.

Step 1009 applies the neighborhood operation to the third ink-density signal corresponding to the input signal set by Step 1008.

Step 1010 stored the result of Step 1009 in the LUT of RAM 202 as a fourth ink-density signal (Y4, M4, C4).

Step 1011 tests if the neighborhood operation has been applied for all input signals. If not, the procedure returns to Step 1008; else the procedure terminates.

Next, the neighborhood operation of Step 1009 is described in the following.

The third ink-density signal is chosen from the result of the first color correction operation and the result of the second color correction operation for the input signal. The second color correction operation obtains an optimal ink-density signal for an input signals unreproduceable by a printer, so that, owing to the shape of the color gamut reproducible by the printer, reproduced colors sometimes suddenly change even if the input signals continuously vary. As a result, the smooth gradation of a reproduced image is damaged. Therefore, the present embodiment performs a three-dimensional spacial filtering in the RGB luminance color space by the neighborhood operation.

FIG. 11 shows an input signal under consideration and 6 neighboring input signals referred in the neighborhood operation in the RGB color space. If the Y component of the third ink-density signal for the input signal under consideration is denoted by Y3(R, G, B), and the Y component of the third ink-density signals for the 6 neighboring input signals are denoted by Y3(R−1, G, B), Y3(R, G−1, B), Y3(R, G, B−1), Y3(R+1, G, B), Y3(R, G+1, B), and Y3(R, G, B+1), then the fourth ink-density signal Y4(R, G, B) for the input signal under consideration is determined by the following neighborhood operation (18).

$$\begin{aligned} Y4(R, G, B) = \{&2 \times Y3(R, G, B) + Y3(R-1, G, B) + \\ &Y3(R, G-1, B) + Y3(R, G, B-1) + \\ &Y3(R+1, G, B) + Y3(R, G+1, B) + \\ &Y3(R, G, B+1)\} \times \tfrac{1}{8} \end{aligned} \tag{18}$$

The M and C components of the fourth ink-density signal are determined by similar operations.

FIGS. 12(*a*) and 12(*b*) show an experimental result of color reproduction by the present embodiment. FIG. 12 (*a*) shows the range of colors reproducible by a printer in u*v* plane of the L*u*v* color space, and FIG. 12 (*b*) shows the encircled part in FIG. 12 (*a*). Target colors and corresponding colors reproduced by a printer by the experiment are plotted in FIG. 12 (*b*), where each small circle indicates a target color, which is unreproduceable by the printer, the triangle connected to the target color with a dotted line indicates the corresponding reproduced color using the third ink-density signal, and the square connected to the target color with a solid line indicates the corresponding reproduced color using the fourth ink-density signal. As observed from FIG. 12 (*b*), the color reproduction using the fourth ink-density signals improves the continuity of color reproduction, when the color reproduction using the third ink-density signals produces unnaturally discontinuous color changes.

The process of determining the ink-density signal for an input signal and results of experiments have been described above for the third embodiment. The present embodiment can suppress sudden changes in color reproduction for continuously changing target colors to reduce discontinuous color reproduction by obtaining an optimal color for each input signal and applying a three-dimensional neighborhood operation in the color space of input signals.

The present embodiment limits the number of input signals to 6 to perform a neighborhood operation. However, the present invention does not limit the number of the third ink-density signals to be used and the coefficients of the formula (18) for a neighborhood operation to those of the present embodiment.

Next, the apparatus of forming color images of the fourth embodiment in accordance with the present invention is described in the following.

The fourth embodiment uses, as its input signal, a Y-corrected luminance signal (r, g, b), each component being an 8-bit signal, and forms color images by a sublimation type thermal transfer printer using inks of cyan, magenta, and yellow.

In the fourth embodiment, the ink-density signals for 32×32×32 representative points, each expressed by the upper 5 bits of each 8-bit component of the input signal (r, g, b), are stored in an LUT (look-up table). The ink-density signal for a point between those representative points is determined by the method of three-dimensional linear interpolation.

Before the composition and operation of the present embodiment is described, the method of interpolation is explained with reference to FIG. 14. FIG. 14 shows a unit cube formed by neighboring 8 representative points Pk, k=0, 1, . . . 7 in the rgb space. For an input signal expressed by a point P inside the cube, the three planes parallel to rg plane, gb plane, and rb plane passing through P divide the cube into 8 rectangular solids, and the volume of the rectangular solid containing the vertex Pk is denoted by Vk. If the ink-density signal of the representative point Pk is (Ck, Mk, Yk), then the ink-density signal of point P is determined by the following interpolation formula (19).

$$C = \sum_{k=0}^{7} Ck \cdot Vk/V \tag{19}$$

$$M = \sum_{k=0}^{7} Mk \cdot Vk/V$$

$$Y = \sum_{k=0}^{7} Yk \cdot Vk/V$$

The composition of the fourth embodiment is described in the following. FIG. 13 shows a block diagram of the apparatus of forming color images in the fourth embodiment.

In FIG. 13, 1301 is an address generator that reads the upper five bits of each component of an input signal (r,g b) and outputs the addresses of the 8 representative points of the unit cube that contains the point expressed by the input signal in synchronous with the CLK signal of the input signal.

1302 is an LUT memory that outputs an 8-bit ink-density signal (Y, M, C) corresponding to an address output from address generator 1302 and a 2-bit COLSEL signal that indicates one of cyan, magenta, and yellow currently being printed. LUT 1302 is configured by a

ROM of 1M bits (128K bytes) and uses an area of 96K bytes.

1303 is a counter that counts up in synchronous with a CLK signal and outputs a 3-bit signal indicating the k of formula (19)

1304 is a weight table memory that memorizes weights Vk/V of (19), reads the lower three bits of the input signal (r, g, b) and the address output from counter 1303, and outputs a weight Vk/V corresponding to the address.

1305 is a calculating means that multiplies each output of LUT memory 1302 by each output of weight table memory 1304, adds up the products in synchronous with the CLK signal to perform the calculation of (19), and outputs an ink-density signal (Y, M, C) to be used in printing.

1306 is a controller that controls the impression energy depending on the ink-density signal output from calculating means 1305.

1307 is a thermal head that impress an ink sheet with heat depending on the impression energy controlled by controller 1307 and forms a full color image on a sheet of paper.

The operation of the apparatus of the present embodiment for printing the first color, i.e. yellow, is described in the following.

First, address generator 1301 successively outputs the addresses of the 8 vertices of the unit cube corresponding to an input signal in synchronous with the CLK signal. Specifically, if the upper 5 bits of the input signal (r, g, b) are (r0, g0, b0), then these addresses are (r0, g0, b0), (r0+1, g0, b0), (r0, g0+1, b0), (r0+1, g0+1, b0), (r0, g0, b0+1), (r0+1, g0, b0+1), (r0, g0+1, b0+1), and (r0+1, g0+1, b0+1). Then LUT memory 1302 outputs the ink-density signals Y0, Y1, . . . , Y7 of yellow corresponding to these addresses.

On the other hand, the lower 3 bits of the input signal (r, g, b) and the output of counter 1303 are provided to weight table 1304, which successively outputs weights V0/V to V7/V.

Then calculating means 1305 calculates formula (19) and outputs the ink-density signal Y of yellow for the input signal (r, g, b).

Controller 1306 controls the impression energy depending on the output signal Y of calculating means 1305, and thermal head 1307 impresses an ink sheet with heat to perform graded printing on a receiving sheet of paper.

After the above operation is performed for printing yellow on the whole receiving sheet of paper, the same operation is performed for magenta, and cyan, so that a graded printing of a full color image is performed on the receiving sheet of paper.

In the present embodiment, the ink-density signals for the 32×32×32 representative points are stored in LUT memory 1302. In order to calculate the ink-density signals, the input signal (r, g, b) for each representative point is converted into a primary-colors signal (R, G, B) by the following (20), and the ink-density signal is obtained from the signal (R, G, B) by the same processing as in the first embodiment.

$$R = r^{2.2}$$

$$G = g^{2.2}$$

$$B = b^{2.2} \qquad (20)$$

In fact, the primary-colors luminance signal (R, G, B) obtained by (20) is converted into a first ink-density signal by (3) to (7) of the first color correction process. Then whether the first ink-density signal is reproducible by the printer or not is judged by the procedure shown in FIG. 3. If the first ink-density signal is reproducible by the printer, then the first ink-density signal is stored in LUT memory 1302. Else, the second ink-density signal determined by the procedure shown in FIG. 5 and operations (9) to (16) is stored in LUT memory 1302.

The composition and operation of the apparatus of forming color images in the fourth embodiment have been described above. The method of forming color images in accordance with the present invention requires operation time for the second color correction operation of determining optimal ink-density signals for input signals unreproduceable by a printer. However, the fourth embodiment stores the ink-density signals in an LUT memory beforehand, so that the ink-density signal is determined by real-time processing for an input signal unreproduceable by a printer. Further, memory size is smaller than in an apparatus storing the ink-density signals for all possible input signals in an LUT memory. As in the first embodiment, color reproduction is performed using optimal available colors for input signals unreproduceable by a printer, so that the present apparatus greatly improves image quality.

Embodiments of the method and apparatus for forming color images in accordance with the present invention have been described above. In each of these embodiment, the input signal is a luminance signal (R, G, B) that drives a CRT, and the first color correction operation is an operation composed of linear operations and nonlinear masking operations. However, the first color correction operation is not limited to that operation. For example, any color correction operation having its inverse such as a prior linear masking operation can be used as the first color correction operation, and the color prediction in the second color correction operation is performed using the inverse of the first color correction operation.

Alternatively, the first color correction operation can be performed by a prior nonlinear masking operation, and the color prediction in the second color correction operation can be performed by a prior linear operation. In this case, color reproduction is performed with high-precision color correction for colors reproducible by a printer, and an optimal color reproduction is performed with color prediction depending on the precision of the linear operation for colors unreproduceable by a printer.

The present embodiments use a sublimation type thermal transfer color printer, but the method and apparatus for forming color images in accordance with the present invention are not limited to the sublimation type thermal transfer color printer.

In this context, the term "ink-density" should be interpreted not in its narrowest meaning but in its widest meaning. Namely, it indicates "toner-density" in the case that color toners are used to reproduce color images.

Further, the interpolation operation for determining an ink-density signal in the fourth embodiment of the present invention employs an 8-point interpolation method, using ratios of volumes, but the present invention does not limit the method of the interpolation to a particular method.

Although the present invention has been fully described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications are apparent to those skilled in the art. Such changes and modifications are to be understood as included within the scope of the present invention as defined by the appended claims unless they depart therefrom.

What is claimed is:

1. A method for forming color images, comprising;
   - a first color correction process for performing a first color correction to an input color signal to obtain a target color chromatically equal to the input color and converting said target color into a first color density signal corresponding to said target color,
   - a judgment process for judging whether or not the input color is reproducible by a printer having a color density,
   - a second color correction process for performing a second color correction to said input color signal when judged in said judgment process that the input color is not reproducible by a printer, said second color correction converting said input color signal into a second color density signal which is visually nearest to said target color within a color gamut reproducible by the printer, said second color correction process including a color reproduction prediction process for predicting colors reproducible by the printer with respect to said target color, a calculation process for calculating evaluation values using at least one evaluation function for evaluating a chromatic relation between each of predicted colors and said target color, and a search process for seeking a best evaluation value among said evaluation values obtained in said calculation process to obtain said second color density signal based on the predicted color giving said best evaluation value, and
   - a color formation process for forming color images while controlling the color density of the printer in accordance with said first color density signal when the input color is judged to be reproducible by the printer and said second color density signal when the input color is judged to be unreproducible by the printer.

2. The method for forming color images according to claim 1 in which the input color is judged to be unreproducible by the printer if one of color components of said first color density signal has a density out of a range defined by a minimum color density equal to that of a print sheet used for printing and a maximum color density reproducible by the printer.

3. The method for forming color image according to claim 1 in which the color density signal to be converted is the first color density signal and said prediction process is performed by inverse operation of the first color density signal to a color signal in a color space of said input color signal.

4. The method for forming color images according to claim 1 wherein a plurality of evaluation functions are provided and used selectively in accordance with color components of said input color signal.

5. The method for forming color images according to claim 4 wherein each of said plurality of evaluation functions E(i)[i=1, . . . , n: n=the total number of a evaluation functions] is given by an equation depicted as

$$E(i)=\{(a_i\Delta L(i)^2+b_i\Delta H_{uv}(i)^2+c_i\Delta S_{uv}(i)^2)/(a(i)+b(i)+c(i))\}^{\frac{1}{2}}$$

wherein

$a(i), b(i), c(i)$: weighing coefficients

$$\Delta L(i) = L_0^* - L(i)^*$$

$$\Delta S_{uv} = S_0 - S(i)$$
$$S_0 = (u_0^{*2} + v_0^{*2})^{\frac{1}{2}}$$
$$S(i) = (u(i)^{*2} + v(i)^{*2})^{\frac{1}{2}}$$

$$\Delta H_{uv} = (S(i) + S_0)\cdot|\theta_0 - \theta(i)|/2$$
$$\theta_0 = \tan^{-1}(v_0^*/u_0^*)$$
$$\theta(i) = \tan^{-1}(v(i)^*/u(i)^*)$$

L_0^*, u_0^*, v_0^* coordinates of the target color in L^*, u^*, v^* space;

$L(i)^*, u(i)^*, v(i)^*$ coordinates of the color to be reproduced.

6. The method for forming color images according to claim 1 wherein a plurality of neighborhood color density signals are calculated from input color signals near to a considered input color signal and the color density signal corresponding to the considered input color signal is corrected by a neighborhood calculation using said plurality of neighborhood color density signals whereby the color density of the printer is controlled by the color density signal corrected by said neighborhood calculation.

7. A color image forming apparatus for controlling a color printer which comprises a first correction means for performing a first color correction to an input color signal using upper bits of said input color signal to obtain a representative point of said input color signal and for converting said representative point of said input color signal into a first color density signal,
   - a judgment means for judging whether or not said representative point of said input color signal is a color reproducible by a printer,
   - a second color correction means for performing a second color correction to said representative point of said input color signal when judged by said judgment means that said representative point of said input color signal is not a color reproducible by the printer, said second color correction converting said representative point of said input color signal into a second color density signal which will reproduce a color visually nearest to said representative point of said input color signal within a color gamut reproducible by the printer,
   - a memory means for storing said first and second color density signals,
   - a memory control means for addressing said memory means using upper bit information of said input color signals and reading the stored color density signal from said memory means, and
   - an interpolation means for performing an interpolation operation to said stored color density signals read from said memory means using lower bit information of said input color information to obtain a final color density signal in response to which the color printer performs color printing operation.

* * * * *

US005874937A

United States Patent [19]

Kesatoshi

[11] Patent Number: 5,874,937

[45] Date of Patent: Feb. 23, 1999

[54] METHOD AND APPARATUS FOR SCALING UP AND DOWN A VIDEO IMAGE

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[73] Assignee: Seiko Epson Corporation, Tokyo, Japan

[21] Appl. No.: 729,300

[22] Filed: Oct. 10, 1996

[30] Foreign Application Priority Data

Oct. 20, 1995 [JP] Japan 7-297578

[51] Int. Cl.^{6} G09G 3/00

[52] U.S. Cl. 345/127; 345/132

[58] Field of Search 345/132, 127, 345/128, 186

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Primary Examiner—Amare Mengistu
Assistant Examiner—Ricardo Osorio
Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

[57] ABSTRACT

An input video image having an arbitrary resolution is converted to another video image having a predetermined resolution of a display device to display the video image with the converted resolution. The frequencies of the synchronizing signals of the input video signal are measured, and then a resolution of an input video signal is determined from the measured frequencies of the synchronizing signals. The video image represented by the input video signal is expanded or contracted, so as to make the resolution of the input video signal coincident with a resolution of the display device. A resulting video image with the converted resolution is displayed on the display device.

12 Claims, 12 Drawing Sheets

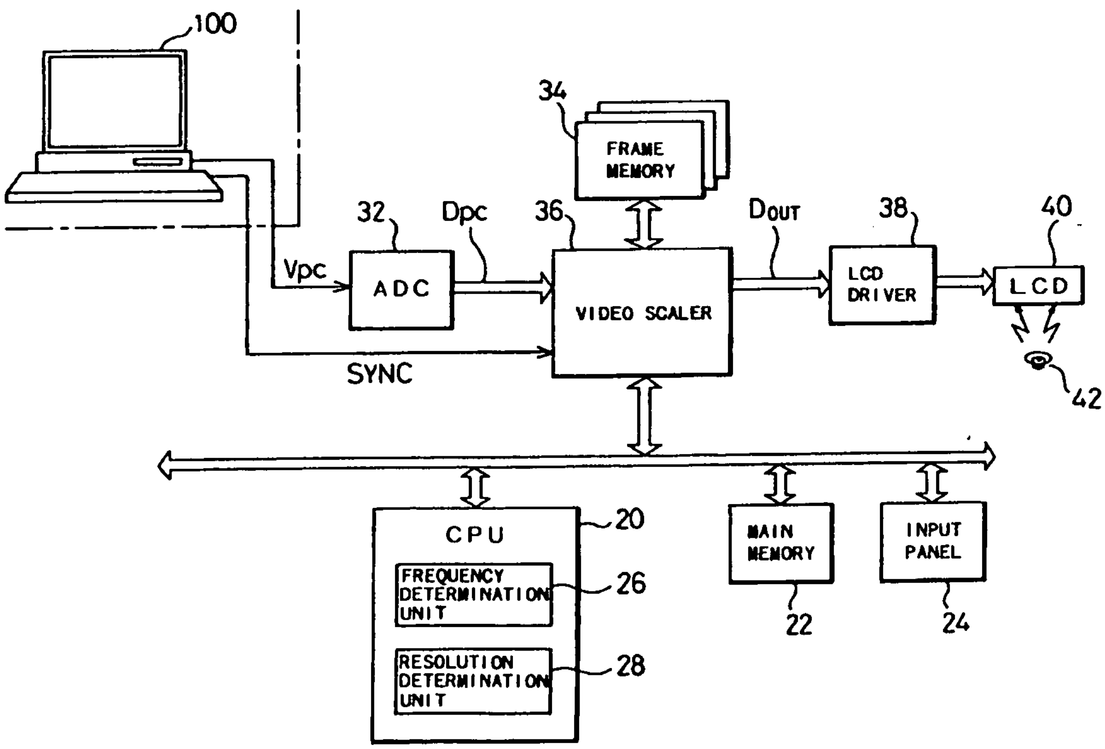
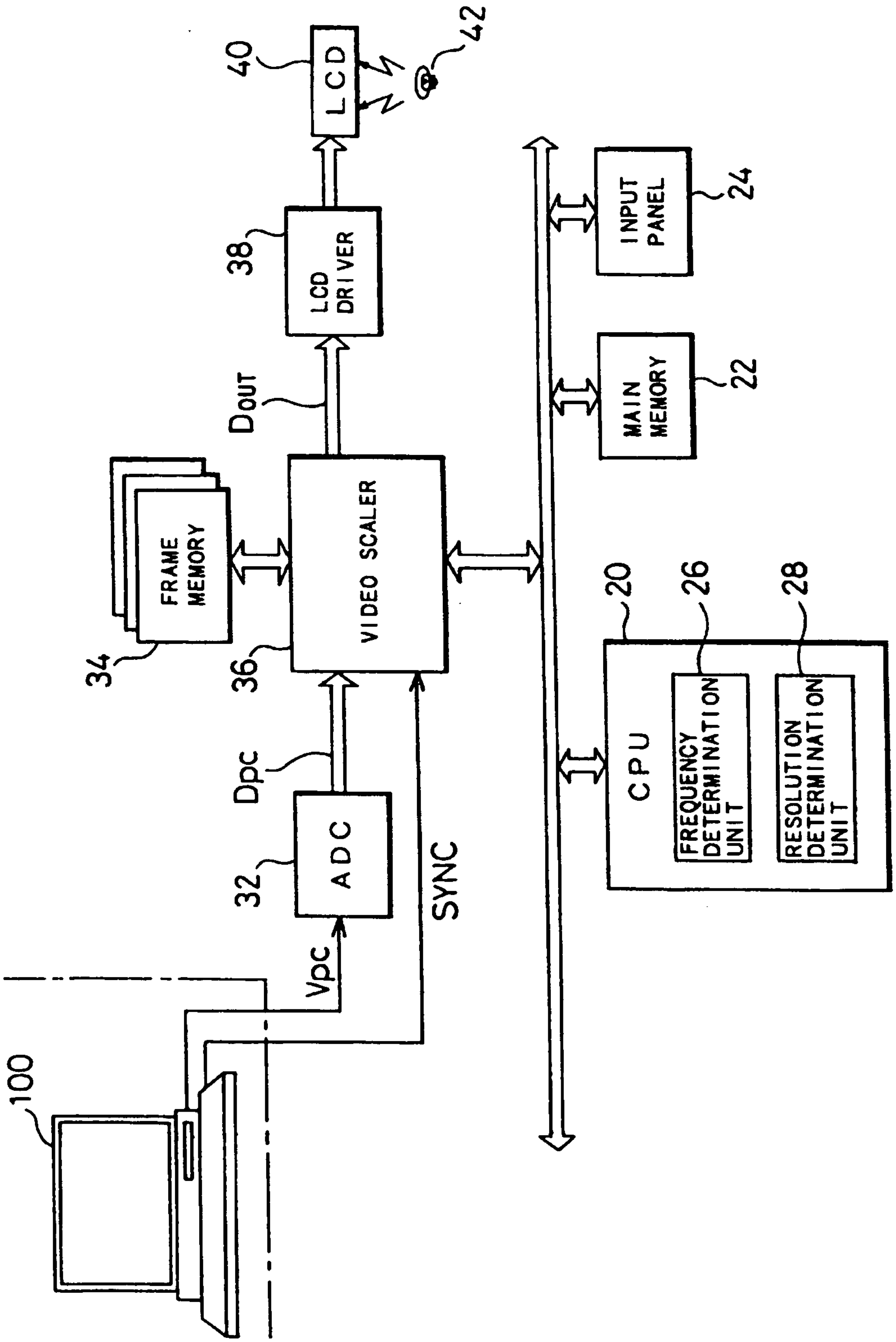
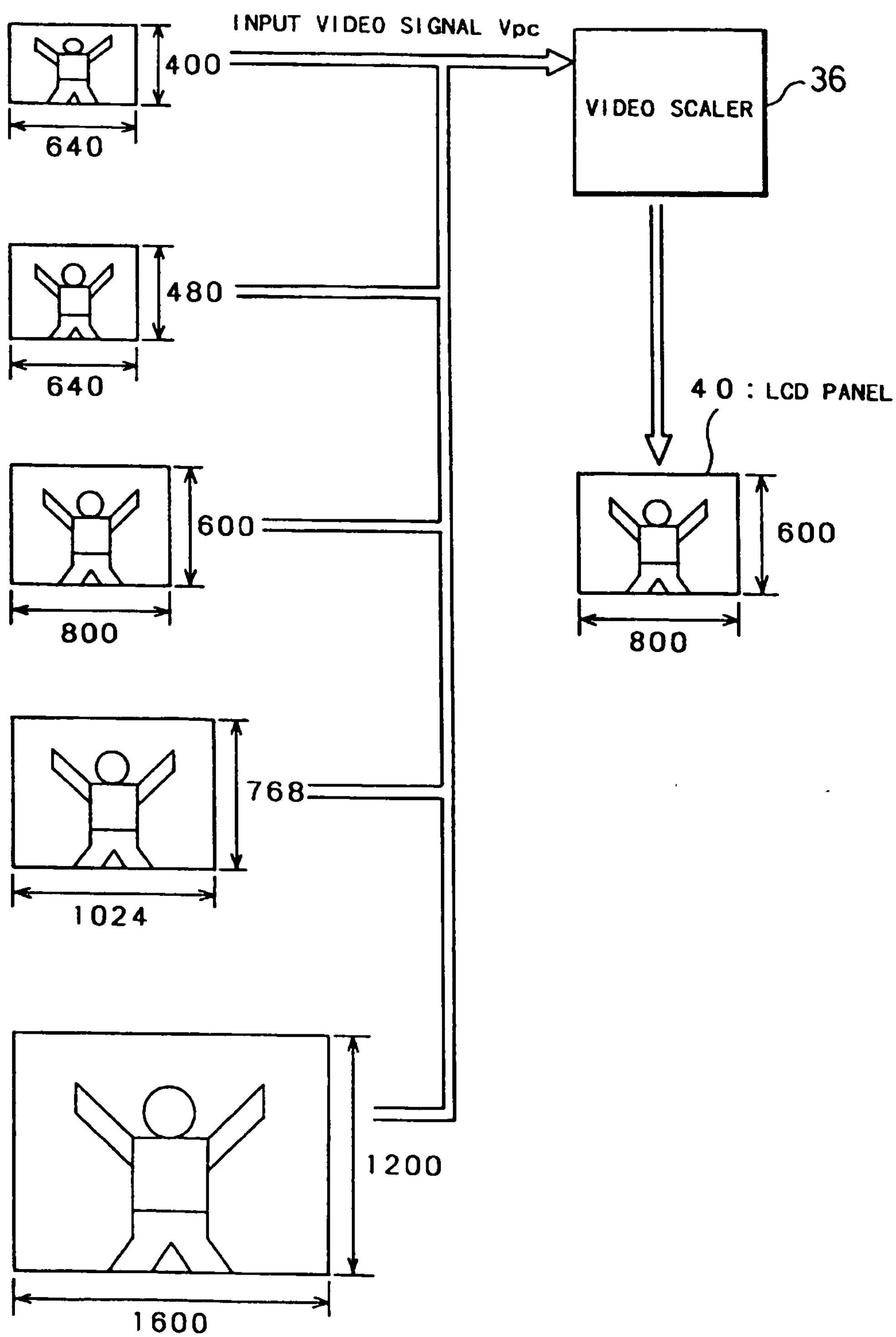


Fig. 1



LCD
40
42
LCD DRIVER
38
INPUT PANEL
24
MAIN MEMORY
22
DOUT
FRAME MEMORY
34
VIDEO SCALER
36
20
26
28
CPU
FREQUENCY DETERMINATION UNIT
RESOLUTION DETERMINATION UNIT
Dpc
ADC
32
SYNC
Vpc
100

Fig. 2


INPUT VIDEO SIGNAL Vpc
400
640
480
640
600
800
768
1024
1200
1600
VIDEO SCALER
36
40 : LCD PANEL
600
800

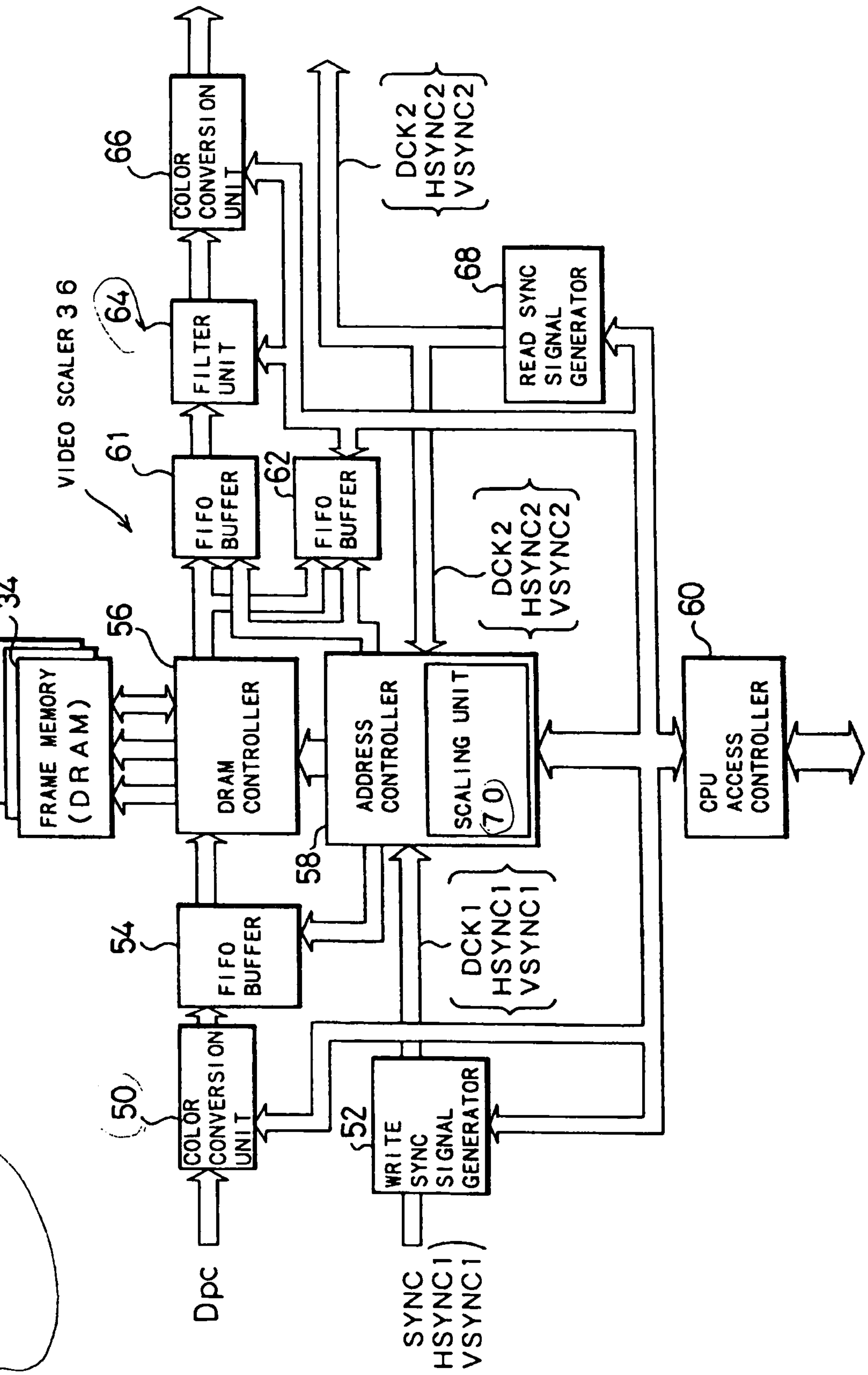

VIDEO SCALER 36
COLOR CONVERSION UNIT
FILTER UNIT
FIFO BUFFER
FIFO BUFFER
FRAME MEMORY (DRAM)
DRAM CONTROLLER
ADDRESS CONTROLLER
SCALING UNIT
READ SYNC SIGNAL GENERATOR
CPU ACCESS CONTROLLER
FIFO BUFFER
COLOR CONVERSION UNIT
WRITE SYNC SIGNAL GENERATOR
DCK2 HSYNC2 VSYNC2
DCK2 HSYNC2 VSYNC2
DCK1 HSYNC1 VSYNC1
Dpc
SYNC (HSYNC1 VSYNC1)
66
64
61
62
68
34
56
58
70
60
54
50
52

Fig. 3

Fig. 4

RESOLUTION DETERMINATION TABLE

RESOLUTIONS (DOTS X LINES)	FREQUENCIES	
	HORIZONTAL (kHz)	VERTICAL (Hz)
640×400	24.8	56.4
640×480	37.5	72
640×480	31.5	60
800×600	48	72
1024×768	56.5	70
1600×1200	61.6	47

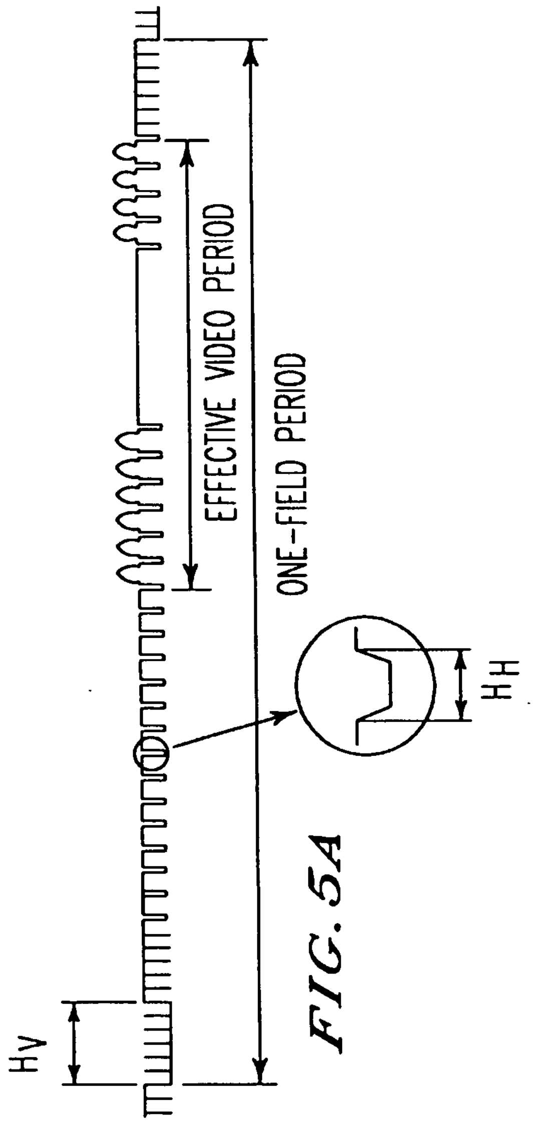
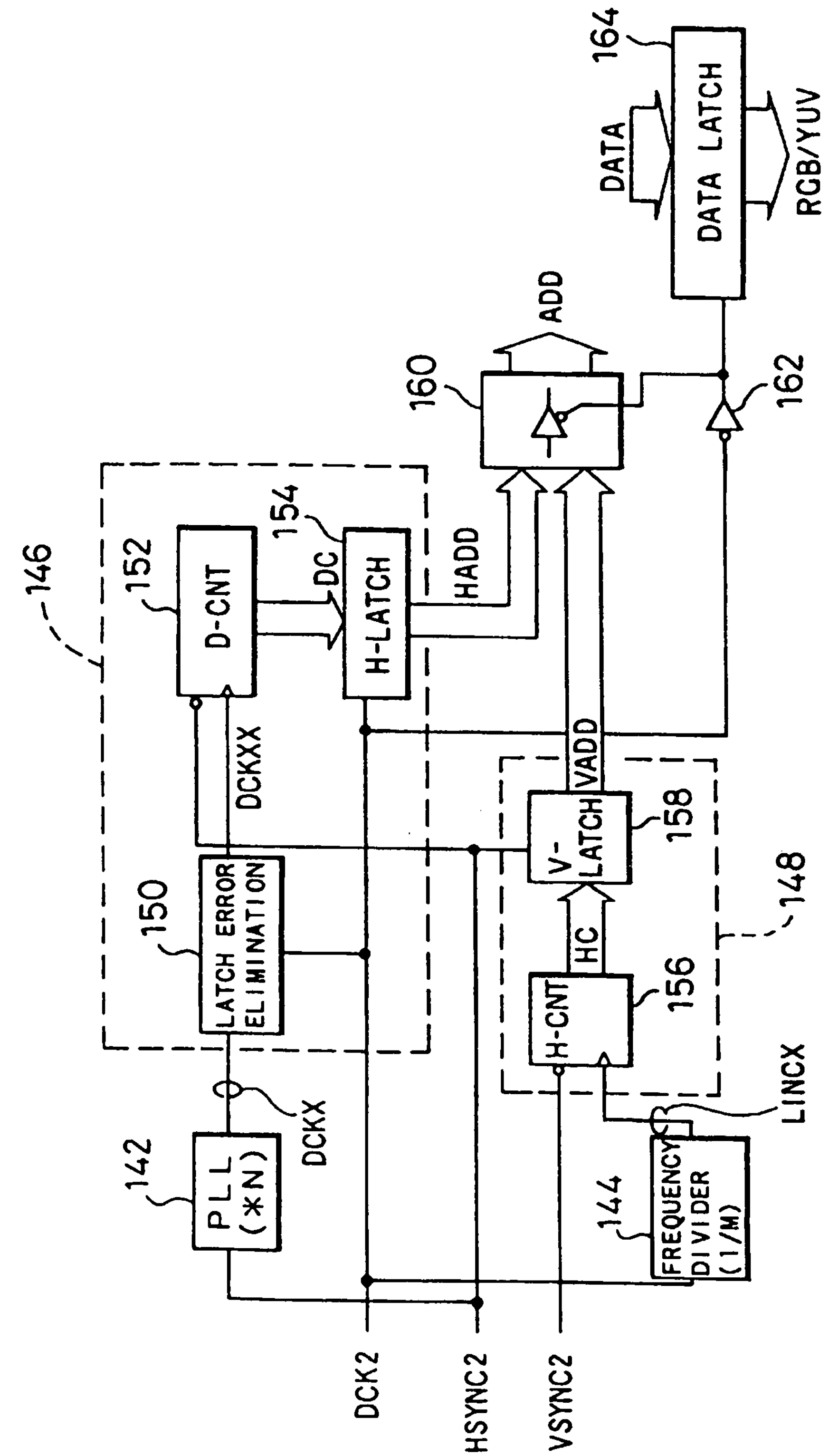


FIG. 5A

FIG. 5B

Fig. 6


164
DATA
DATA LATCH
RGB/YUV
ADD
160
162
146
152
D-CNT
154
DC
H-LATCH
HADD
DCKXX
VADD
158
V-LATCH
148
150
LATCH ERROR ELIMINATION
HC
H-CNT
156
142
PLL (*N)
DCKX
LINCX
144
FREQUENCY DIVIDER (1/M)
DCK2
HSYNC2
VSYNC2

VERTICAL MAGNIFICATION : M V2 = $\frac{fHSYNC2}{fLINCX}$

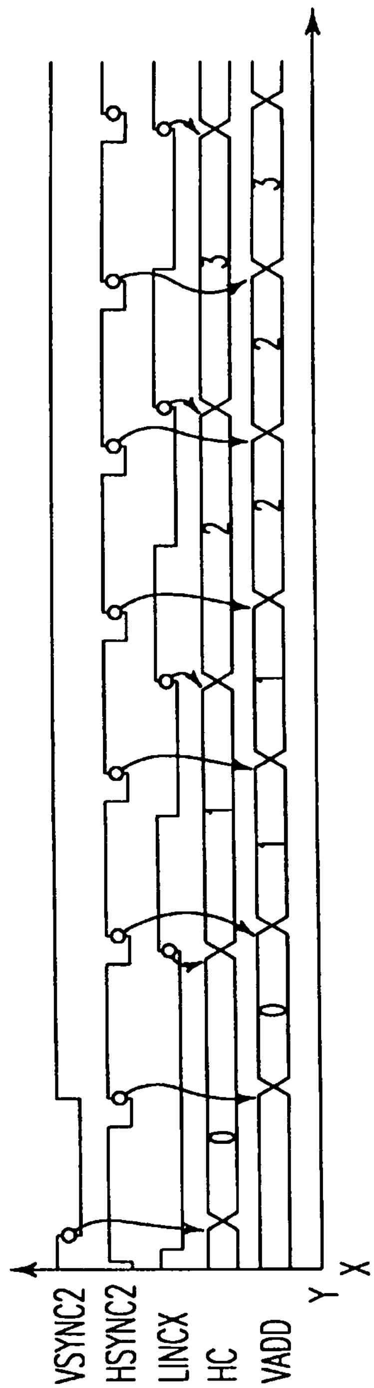


FIG. 7A
FIG. 7B
FIG. 7C
FIG. 7D
FIG. 7E

Fig. 8A

HORIZONTAL ADDRESSES HADD

VERTICAL ADDRESSES VADD

	0	1	2	3	4
0	12	34	56	78	90
1	34	56	78	90	12
2	56	78	90	12	34
3	78	90	12	34	56
4	90	12	34	56	78

VIDEO DATA IN FRAME MEMORY 34

Fig. 8B

	0	0	1	2	2	3	4	4
0	12	12	34	56	56	78	90	90
1	34	34	56	78	78	90	12	12
1	34	34	56	78	78	90	12	12
2	56	56	78	90	90	12	34	34
2	56	56	78	90	90	12	34	34
3	78	78	90	12	12	34	56	56
4	90	90	12	34	34	56	78	78
4	90	90	12	34	34	56	78	78

EXPANDED VIDEO DATA

HORIZONTAL MAGNIFICATION : $MH2 = \frac{fDCK2}{fDCKX}$

VERTICAL MAGNIFICATION : $MV2 = \frac{fHSYNC2}{fLINCX}$

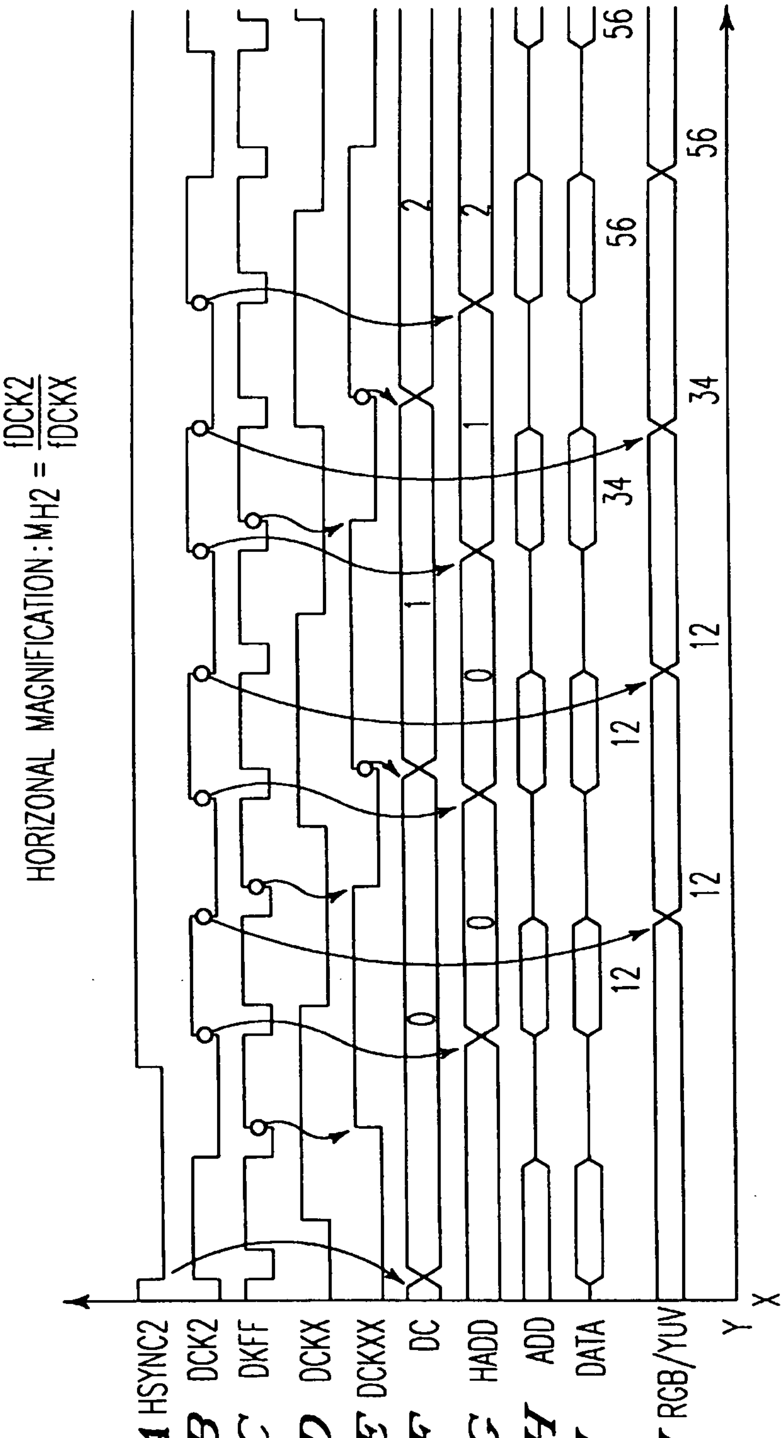


FIG. 9A
FIG. 9B
FIG. 9C
FIG. 9D
FIG. 9E
FIG. 9F
FIG. 9G
FIG. 9H
FIG. 9I
FIG. 9J

Fig. 10

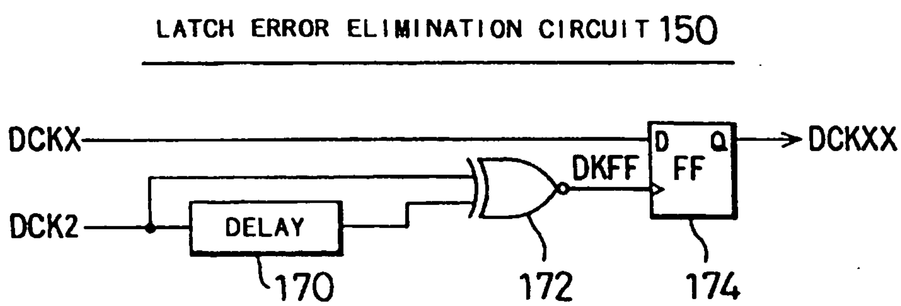
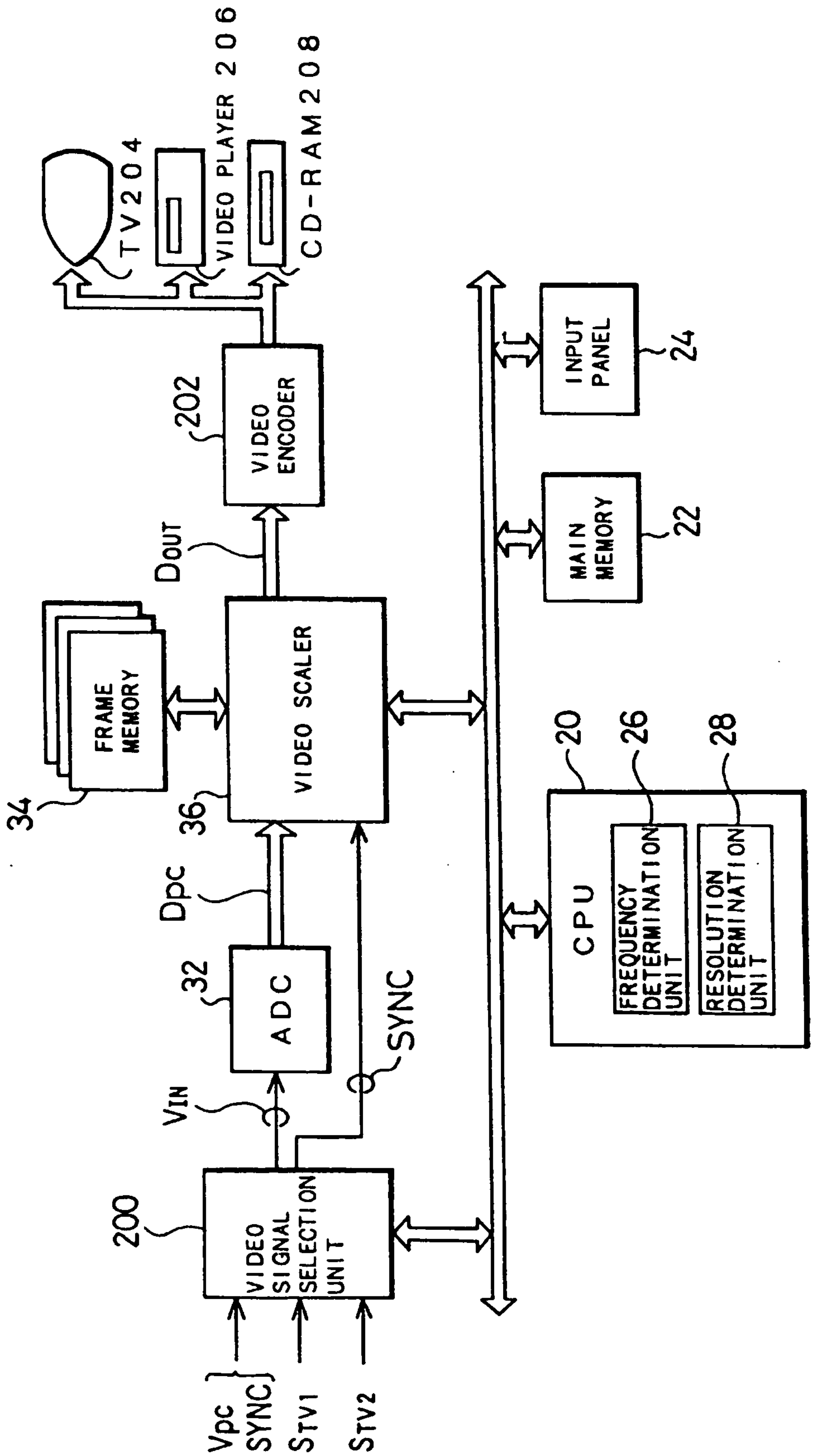

LATCH ERROR ELIMINATION CIRCUIT 150
DCKX
DCK2
DELAY
170
DKFF
172
D
Q
FF
174
DCKXX

Fig. 11


TV204
VIDEO PLAYER 206
CD-RAM 208
202
VIDEO ENCODER
DOUT
FRAME MEMORY
34
VIDEO SCALER
36
INPUT PANEL
24
MAIN MEMORY
22
20
26
28
CPU
FREQUENCY DETERMINATION UNIT
RESOLUTION DETERMINATION UNIT
DPC
32
ADC
SYNC
VIN
200
VIDEO SIGNAL SELECTION UNIT
Vpc
SYNC
STV1
STV2

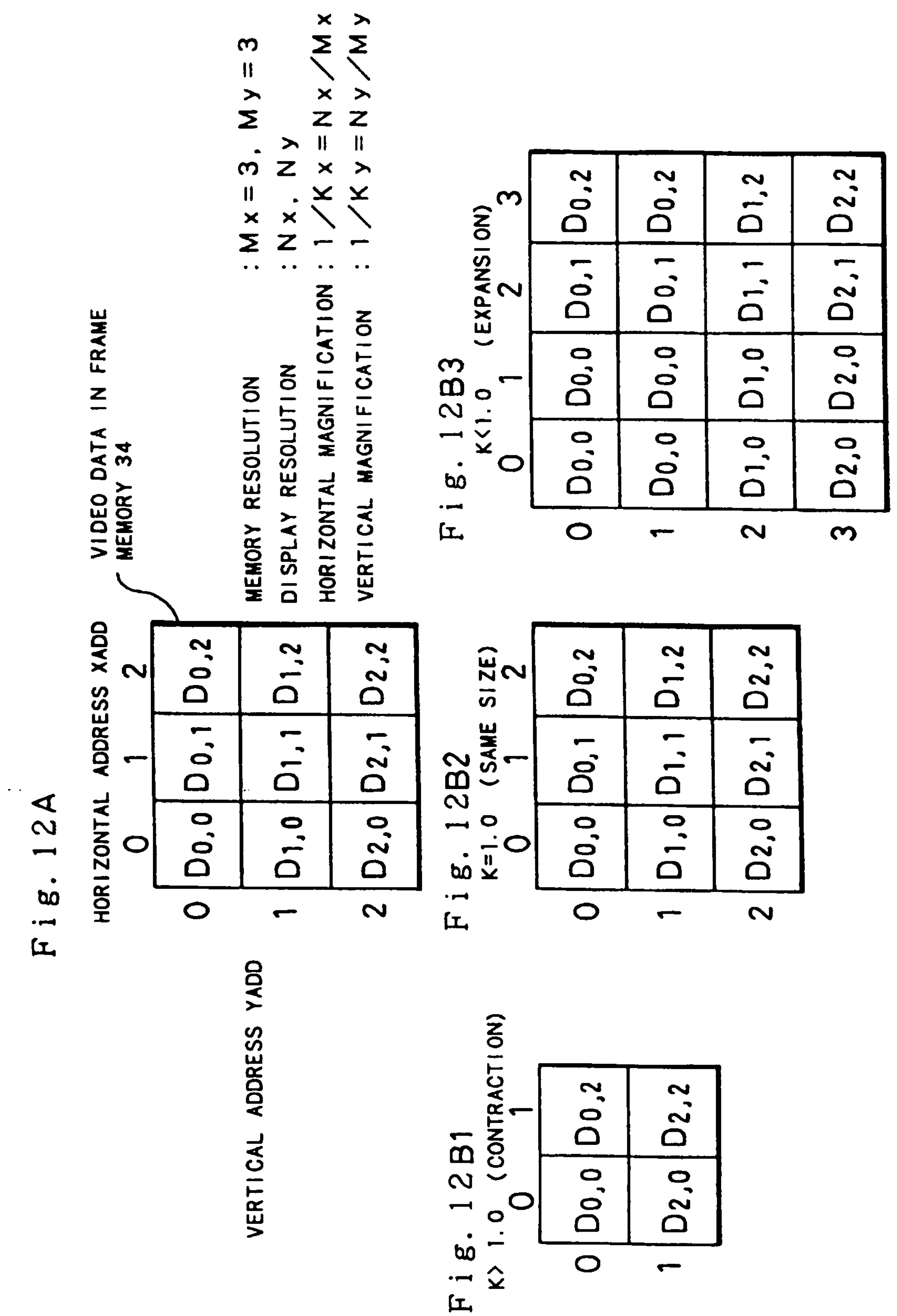


Fig. 12A
HORIZONTAL ADDRESS XADD
VERTICAL ADDRESS YADD
VIDEO DATA IN FRAME MEMORY 34
D0,0 D0,1 D0,2
D1,0 D1,1 D1,2
D2,0 D2,1 D2,2
MEMORY RESOLUTION : Mx = 3, My = 3
DISPLAY RESOLUTION : Nx, Ny
HORIZONTAL MAGNIFICATION : 1/Kx = Nx/Mx
VERTICAL MAGNIFICATION : 1/Ky = Ny/My
Fig. 12B1
K> 1.0 (CONTRACTION)
D0,0 D0,2
D2,0 D2,2
Fig. 12B2
K=1.0 (SAME SIZE)
D0,0 D0,1 D0,2
D1,0 D1,1 D1,2
D2,0 D2,1 D2,2
Fig. 12B3
K<1.0 (EXPANSION)
D0,0 D0,0 D0,1 D0,2
D0,0 D0,0 D0,1 D0,2
D1,0 D1,0 D1,1 D1,2
D2,0 D2,0 D2,1 D2,2

METHOD AND APPARATUS FOR SCALING UP AND DOWN A VIDEO IMAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of and an apparatus for scaling up and down an input video image and displaying the resultant video image on a display device.

2. Description of the Related Art

In some cases, it is required to display video images generated by a computer on another display device, such as a liquid-crystal projector. In such a case, the computer should generate video signals according to the resolution of the display device. In the description of this specification, the term "resolution" implies both a number of dots (that is, a number of pixels) in a horizontal direction of a video image and a number of lines (that is, a number of scanning lines) in a vertical direction. The number of dots in the horizontal direction is referred to as the horizontal resolution, whereas the number of lines in the vertical direction is referred to as the vertical resolution.

The resolution and the number of tones of a video image generated by a computer are restricted by the capacity of a video RAM (VRAM) in the computer. The number of tones is reduced for a display with a greater resolution (that is, a larger screen size), and increased for a display with a smaller resolution. When the display device has a significantly large screen size, it may be impossible to make the resolution of a video signal generated by the computer coincident with the resolution of the display device. The similar problem arises when a video image generated by a device other than the computer (for example, a television image) is displayed on a display device other than a television receiver.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to convert any resolution of an input video image to a resolution of a display device and display the video image with the converted resolution.

The present invention is directed to a video image scaling apparatus for scaling up or down an input video image and displaying the scaled video image on a display device. The apparatus comprises: resolution determination means for analyzing an input video signal to determine a resolution of the input video signal; and scaling means for expanding or contracting a video image expressed by the input video signal so that the resolution of the video signal is made equal to a resolution of the display device.

Since the resolution of a display device is known, a ratio of the resolution of the input video signal to the resolution of the display device can be obtained if the resolution of the input video signal is determined. Expansion or contraction of a video image by the ratio will make the resolution of a video signal equal to the resolution of the display device.

In a preferred embodiment of the present invention, the resolution determination means comprises: resolution storage means for storing relations between the resolution of the input video signal and frequencies of synchronizing signals of the input video signal; frequency determination means for determining frequencies of the synchronizing signals of the input video signal; and means for reading out a resolution corresponding to the frequencies of the synchronizing signals from the resolution storage means.

When the relations between the resolutions of a video signal and frequencies of synchronizing signals are stored in the resolution storage means, the resolution can be readily determined according to the frequencies of the synchronizing signals.

In accordance with an aspect of the present invention, the apparatus further comprises: means for displaying a sign indicating that a resolution is unknown when the frequencies of the synchronizing signals of the input video image are not stored in the resolution storage means; and resolution setting means for setting a value of the unknown resolution of the input video signal and registering a relation between the resolution and the frequencies of the synchronizing signals of the input video signal in the resolution storage means.

This aspect allows to convert the resolution of an input image signal even if the input video signal has synchronizing signals of unknown frequencies.

The scaling means comprises: a first buffer memory for temporarily storing the input video signal; a frame memory in which a video signal read out of the first buffer memory is written; a second buffer memory for temporarily storing a video signal read out of the frame memory; and memory control means for giving a write address to the frame memory while successively reading out video signals from the first buffer memory to write the video signal read out of the first buffer memory into the frame memory, and for giving a read address to the frame memory to read out the video signal from the frame memory and transfer the video signal to the second buffer memory, and wherein the memory control means comprises: means for expanding or contracting a video image read out of the frame memory by adjusting the read address given to the frame memory.

The present invention is also directed to a method of scaling up or down an input video image and displaying the scaled video image on a display device. The method comprises the steps of: (a) analyzing an input video signal to determine a resolution of the input video signal; and (b) expanding or contracting a video image expressed by the input video signal so that the resolution of the video signal is made equal to a resolution of the display device.

These and other objects, features, aspects, and advantages of the present invention will become more apparent from the following detailed description of the preferred embodiments with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the structure of a liquid-crystal projector as a first embodiment according to the present invention;

FIG. 2 schematically illustrates functions of a video scaler 36;

FIG. 3 is a block diagram illustrating the internal structure of the video scaler 36;

FIG. 4 shows the contents of a resolution determination table;

FIG. 5 shows a wave form of a composite video signal;

FIG. 6 is a block diagram illustrating the internal structure of a scaling unit 70;

FIG. 7 is a timing chart showing a process of generating vertical addresses;

FIGS. 8A and 8B show a concrete procedure of expanding a video image;

FIG. 9 is a timing chart showing a process of generating horizontal addresses;

FIG. 10 is a block diagram illustrating the internal structure of a latch error elimination circuit 150;

FIG. 11 is a block diagram illustrating the structure of a down converter as a second embodiment according to the present invention; and

FIGS. 12A, 12B1, 12B2, and 12B3 show a process of expanding and contracting a video image by multiplying read addresses by a predetermined coefficient K.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a block diagram illustrating the structure of a liquid-crystal projector as a first embodiment according to the present invention. The liquid-crystal projector projects video images generated by a personal computer **100** on a large-size screen (not shown). The liquid-crystal projector includes a CPU **20**, a main memory **22**, an input panel **24** functioning as input means, an A-D converter **32**, a frame memory **34**, a video scaler **36**, LCD drivers **38**, LCD panels (liquid-crystal panels) **40**, and a light source **42**. The frame memory **34** includes three memory planes for storing R, G, and B signals, respectively. The LCD drivers **38** and the LCD panels are also provided for the R, G, and B signals.

The CPU **20** functions as a frequency determination unit **26** for determining a frequency of a synchronizing signal SYNC given by the personal computer **100** and as a resolution determination unit **28** for determining a resolution corresponding to the frequency of the synchronizing signal SYNC. The CPU **20** executes computer program codes stored in the main memory **22** to implement these functions.

The A-D converter **32** converts an analog video signal VPC generated by the personal computer **100** to a digital video signal DPC and transmits the digital video signal DPC to the video scaler **36**. The video scaler **36** receives the digital video signal DPC as well as the synchronizing signal SYNC output from the personal computer **100**. In the description of this specification, the term "video signals" may represent video signals in a narrow sense that do not include synchronizing signals, and also those in a broad sense that include synchronizing signals.

The video scaler **36** writes the input digital video signal DPC into the frame memory **34** while reading out a video signal from the frame memory **34** and supplying the video signal to the LCD driver **38**. In the course of writing or reading procedure, the video scaler **36** expands or contracts a video image, so as to make the resolution of the video signal coincident with a standard resolution of the LCD panel **40**. The LCD driver **38** reproduces a video images that is transmitted from the video scaler **36** on the LCD panel **40**. The video images reproduced on the LCD panels **40** are finally projected as a color image on the screen by means of an optical system including the light source **42**.

FIG. 2 schematically illustrates the functions of the video scaler **36**. As shown in the left half of FIG. 2, video images generated by the personal computer **100** may have a variety of resolutions (for example, 640 dots by 400 lines, 640 dots by 480 lines, 800 dots by 600 lines, 1,024 dots by 768 lines, and 1,600 dots by 1,200 lines). The standard resolution of the LCD panel **40** is, on the other hand, fixed to a predetermined value. In the example of FIG. 2, the standard resolution is 800 dots by 600 lines. The video scaler **36** accordingly expands or contracts the input video signal VPC in order to generate a video signal having the standard resolution of the LCD panel **40**. When the video signal VPC generated by the personal computer **100** is input into the liquid-crystal projector of this embodiment, a video image expressed by the video signal VPC will be reproduced on the whole screen of the LCD panels **40**. This means that the resolution in the liquid-crystal projector is independent of the resolution of the input video signal VPC. Accordingly, a video image originally generated by the personal computer **100** can be reproduced on the LCD panel **40** to cover its whole display area regardless of the resolution and the number of tones of the image which are determined by the personal computer **100**.

FIG. 3 is a block diagram illustrating the internal structure of the video scaler **36**. The video scaler **36** includes a first color conversion unit **50**, a write synchronizing signal generator **52**, an input FIFO buffer **54**, a DRAM controller **56**, an address controller **58**, a CPU access controller **60**, two output FIFO buffers **61** and **62**, a filter unit **64**, a second color conversion unit **66**, and a read synchronizing signal generator **68**. As shown in FIG. 3, the frame memory **34** is constructed as a dynamic RAM in this embodiment. The DRAM controller **56** is a circuit for controlling a process of writing video signals into the frame memory **34** and a process of reading out video signals from the frame memory **34**.

The digital video signal DPC output from the A-D converter **32** shown in FIG. 1 is given to the first color conversion unit **50**, which carries out a color conversion to RGB signals, if necessary. By way of example, when the input digital video signal DPC is an YCrCb signal, the first color conversion unit **50** converts the YCrCb signal to an RGB signal.

The synchronizing signal SYNC generated by the personal computer **100** includes a horizontal synchronizing signal HSYNC1 and a vertical synchronizing signal VSYNC1. The write synchronizing signal generator **52** has an internal PLL circuit (not shown), which multiplies the frequency of either the horizontal synchronizing signal HSYNC1 or the vertical synchronizing signal VSYNC1 by N_0 to generate a dot clock signal DCK1. The dot clock signal DCK1 indicates an update timing of a dot position in the horizontal direction. The dot clock signal DCK1 as well as the horizontal synchronizing signal HSYNC1 and the vertical synchronizing signal VSYNC1 are supplied to the address controller **58**.

The video signal converted by the first color conversion unit **50** is temporarily stored in the FIFO buffer **54** and written into the frame memory **34** by the DRAM controller **56**. The FIFO buffer **54** works to adjust the timing of the writing operation. The writing operation into the frame memory **34** is carried out synchronously with the write synchronizing signals (DCK1, HSYNC1, and VSYNC1) output from the write synchronizing signal generator **52**. Each dot position (or horizontal address) is updated synchronously with the dot clock signal DCK1, while each scanning line position (vertical address) is updated synchronously with the horizontal synchronizing signal HSYNC1. Each frame or each field is updated synchronously with the vertical synchronizing signal VSYNC1. The DRAM controller **56** also reads out video signals stored in the frame memory **34** and writes the input video signals alternately into the two FIFO buffers **61** and **62**. The reading-out operation from the frame memory **34** is carried out synchronously with read synchronizing signals (DCK2, HSYNC2, and VSYNC2) generated by the read synchronizing signal generator **68**. The read synchronizing signals (DCK2, HSYNC2, and VSYNC2) are also supplied to the LCD driver **38** to be used as display synchronizing signals for the LCD panel **40**. The address controller **58** is a circuit for generating a write address and a read address and supplying the write and read addresses to the DRAM controller **56**. The address controller **58** further includes a scaling unit **70** for expanding or contracting (or scaling up or down) a video image.

One line of video signals read out from the frame memory **34** are written alternately into the two output FIFO buffers **61** and **62**. In the mean time, video signals are read out from the buffer which is not under the writing operation, to be supplied to the filter unit **64**. The filter unit **64** is a circuit for carrying out a variety of filtering processes, such as γ correction (conversion of input/output tones) and left-to-right and top-to-bottom inversions of video images. The filtered video signal undergoes the color conversion in the second color conversion unit **66**, if necessary, to be converted to an output video signal DOUT. The output video signal DOUT is then supplied to the LCD driver **38** (see FIG. **1**).

The CPU **20** shown in FIG. **1** has access to the respective elements in the video scaler **36** via the CPU access controller **60** shown in FIG. **3**. In measuring the frequency of the synchronizing signal SYNC corresponding to the input video signal VPC, the CPU **20** receives the signals output from the write synchronizing signal generator **52** via the CPU access controller **60**. The CPU **20** first functions as the frequency determination unit **26** (see FIG. **1**) to measure the frequencies of the horizontal synchronizing signal HSYNC1 and the vertical synchronizing signal VSYNC1, which are supplied to the write synchronizing signal generator **52**. The CPU **20** then functions as the resolution determination unit **28** to determine the resolution of the input video image VPC based on the measured frequencies.

FIG. **4** shows a resolution determination table indicating relations between the resolutions and the frequencies of the synchronizing signals. The relations between the various resolutions (the number of dots by the number of lines) and the frequencies of the horizontal synchronizing signal and the vertical synchronizing signal are registered in the resolution determination table, which is stored in the main memory **22**. The frequency of an operation clock of the CPU **20** is at least tens of MHz while the frequency of the horizontal synchronizing signal is tens of kHz, and the frequency of the vertical synchronizing signal several is tens of Hz. The CPU **20** can thus execute the computer program codes to implement the function of the frequency determination unit **26** to measure these frequencies with a sufficiently high accuracy. In accordance with a concrete procedure, the CPU **20** carries out the counting-up operation at a regular interval and obtains a count between edges (such as falling edges) of the horizontal synchronizing signal HSYNC1. The CPU **20** then calculates the frequency of the horizontal synchronizing signal HSYNC1 from the count. The frequency of the vertical synchronizing signal VSYNC1 can be determined in a similar manner. After determining the frequencies of the synchronizing signals HSYNC1 and VSYNC1, the resolution determination unit **28** determines the corresponding resolution by referring to the resolution determination table (FIG. **4**).

As shown in FIG. **4**, plural combinations of the frequencies of synchronizing signals may correspond to an identical resolution. It is accordingly desirable to register relations between the resolutions and the frequencies used in a number of commercially available apparatuses as many as possible into the resolution determination table. There is, however, still a possibility of receiving a video signal having a frequency not registered in the resolution determination table. In such a case, the CPU **20** shown in FIG. **1** may make a display on the LCD panel **40** (or on a display unit of the input panel **24**), showing that the frequency of the input video signal VPC has not yet been registered. The user then sets the resolution (the number of dots by the number of lines) of the input video signal VPC with the input panel **24**, thereby registering the relation between the frequency and the resolution into the resolution determination table. In order to realize this process, it is desirable to store the resolution determination table in a write-enable memory, such as a RAM or a flash memory.

The resolution of the input video signal VPC may be determined on the basis of not only the frequencies of the horizontal synchronizing signal and the vertical synchronizing signal but on period widths H_H and H_V of the horizontal and vertical synchronizing signals and on the kind of interlacing. FIG. **5** shows the period widths H_H and H_V of the horizontal synchronizing signal and the vertical synchronizing signal. For convenience of illustration, FIG. **5** shows a wave form of a composite video signal. Determination of the resolution of the input video signal based on the frequencies of the synchronizing signals as well as their period widths H_H and H_V and the state of interlacing can effectively reduce the possible errors that may be made in the determination.

The horizontal resolution and the vertical resolution determined by the resolution determination unit **28** are given to the address controller **58** via the CPU access controller **60** (see FIG. **3**). The scaling unit **70** in the address controller **58** carries out expansion or contraction of a video image as described before along with FIG. **2**, in order to convert the horizontal and vertical resolutions to the standard resolutions of the LCD panel **40**.

FIG. **6** is a block diagram illustrating the internal structure of the scaling unit **70**. The scaling unit **70** includes a PLL circuit **142**, a frequency divider **144**, a horizontal address generator **146**, a vertical address generator **148**, a 3-state buffer **160**, and an inverter **162**. A data latch **164** shown in FIG. **6** is a circuit included in the DRAM controller **56**. The horizontal address generator **146** includes a latch error elimination circuit **150**, a first counter **152**, and a first latch **154**. The vertical address generator **148** includes a second counter **156** and a second latch **158**.

The PLL circuit **142** receives the horizontal synchronizing signal HSYNC2, which is generated for the reading-out operation, and generates a second dot clock signal DCKX having the frequency of N times the frequency of HSYNC2. The frequency divider **144** receives the dot clock signal DCK2, which is also generated for the reading operation, and divides the frequency of DCK2 by M to generate a line increment signal LINCX. The preset values N and M in the PLL circuit and the frequency divider **144** are used to convert the resolution of the input video signal VPC to the resolution of the LCD panel **40**, and are respectively determined by the CPU **20**. A concrete process of determining the preset values N and M will be described later.

FIG. **7** is a timing chart showing operation of the vertical address generator **148**. After being reset by the vertical synchronizing signal VSYNC2 for the reading operation (FIG. **7**(*a*)), the second counter **156** counts the number of pulses in the line increment signal LINCX. A count HC on the second counter **156** (FIG. **7**(*d*)) is latched at a rising edge of the horizontal synchronizing signal HSYNC2 and given as a vertical address VADD to the 3-state buffer **160**. In the example of FIG. **7**(*e*), the vertical address VADD is updated as 0, 1, 1, 2, . . .

FIGS. **8**A and **8**B show a concrete process of expanding a video image. FIG. **8**A shows video data stored in the frame memory **34**, and FIG. **8**B shows expanded video data. Numerals written in the tables represent the values of video data. In the timing chart of FIG. **7**(*e*), video data are read out from the frame memory **34** such that: a video image on a scanning line of VADD=0 is read out once, a video image on

a scanning line of VADD=1 twice, a video image on a scanning line of VADD=2 twice, and the like. The video image thus read out is accordingly expanded in the vertical direction as shown in FIG. 8B. A vertical magnification MV2 is given as a ratio of a frequency fHSYNC2 of the horizontal synchronizing signal HSYNC2 to a frequency fLINCX of the line increment signal LINCX. The video image can be expanded by an arbitrary magnification in the vertical direction by adjusting the preset value M in the frequency divider 144 (FIG. 6). The video image will be contracted in the vertical direction when the value of the magnification MV2 is less than 1.

FIG. 9 is a timing chart showing an operation of the horizontal address generator 146. The latch error elimination circuit 150 (FIG. 6) generates a third dot clock signal DCKXX (FIG. 9(*e*)) from the first and the second dot clock signals DCK2 and DCKX (FIGS. 9(*b*) and 9(*d*)).

FIG. 10 is a block diagram illustrating the internal structure of the latch error elimination circuit 150. The latch error elimination circuit 150 includes a delay circuit 170, an exclusive NOR (EXNOR) circuit 172, and a D-type flip-flop 174. An output signal DKFF of the EXNOR circuit 172 is an inversion of an exclusive OR of the first dot clock signal DCK2 and a signal obtained by delaying the dot clock signal DCK2 by a predetermined time period. The signal DKFF thus represents timings of rises and falls of the first dot clock signal DCK2 as shown in FIG. 9(*c*).

The output signal DKFF of the EXNOR circuit 172 is supplied to a clock input terminal of the flip-flop 174, while the second dot clock signal DCKX is given to a D-input terminal of the flip-flop 174. The third dot clock signal DCKXX output from the flip-flop 174 thus represents the level of the second dot clock signal DCKX at a rising edge of the output signal DKFF of the EXNOR circuit 172 as shown in FIG. 9(*e*). The third dot clock signal DCKXX has the frequency identical with that of the second dot clock signal DCKX. The output signal DKFF of the EXNOR circuit 172 rises after a predetermined delay time from an edge of the first dot clock signal DCK2, and the timing of the level change of the third dot clock signal DCKXX is delayed by the predetermined delay time from the edge of the first dot clock signal DCK2 accordingly. The latch error elimination circuit 150 generates the third dot clock signal DCKXX, in order to prevent the value of a horizontal address latched by the first latch 154 from being unstable as discussed later in detail.

After being reset by the pulse of the horizontal synchronizing signal HSYNC2, the first counter 152 of the horizontal address generator 146 (FIG. 6) counts up the number of pulses of the third dot clock signal DCKXX generated by the latch error elimination circuit 150 and supplies a count DC (FIG. 9(*f*)) to the first latch 154. Since the third dot clock signal DCKXX and the second dot clock signal DCKX have identical frequencies as mentioned above, the count DC of the first counter 152 practically indicates the number of pulses of the second dot clock signal DCKX. The first latch 154 latches the count DC synchronously with the first dot clock signal DCK2, and gives the latched count as a horizontal address HADD (FIG. 9(*g*)) to the 3-state buffer 160. The horizontal address HADD accordingly represents the number of pulses of the second dot clock signal DCKX and is updated at every rising edge of the first dot clock signal DCK2. The value of the horizontal address HADD can be updated in a predetermined manner by adjusting a frequency fDCK2 of the first dot clock signal DCK2 and a frequency fDCKX of the second dot clock signal DCKX. In the example of FIG. 9(*g*), the value of the horizontal address HADD is varied as 0,0,1, . . .

The tables of FIGS. 8A and 8B discussed above show a process of expanding a video image according to the horizontal address HADD in FIG. 9(*g*). The timing chart shown in FIG. 9 corresponds to timings of generating addresses in the horizontal direction on an upper-most scanning line having the vertical address of VADD=0. The horizontal address HADD is updated as 0,0,1 . . . as shown in FIG. 9(*g*). Video data of the respective pixels existing on this scanning line are successively read out from the frame memory 34 o that the video data of the pixel having the horizontal address HADD=0 is read out twice, the video data of the pixel having the horizontal address HADD=1 is read out once, and the like.

As discussed above, the horizontal address HADD depends upon the relation between the frequencies of the two dot clock signals DCK2 and DCKX. A video image can thus be expanded or contracted in the horizontal direction by adjusting the frequencies of these dot clock signals DCK2 and DCKX. A magnification MH2 of a video image in the horizontal direction is given as the ratio of the frequency fDCK2 of the first dot clock signal DCK2 to the frequency fDCKX of the second dot clock signal DCKX as shown in the bottom of FIG. 8. A video image can accordingly be expanded or contracted by an arbitrary magnification in the horizontal direction by adjusting the preset value N in the PLL circuit 142.

The reason why the latch error elimination circuit 150 is used to generate the signal DCKXX is as follows. As shown in FIG. 9(*f*), the count DC on the first counter 152 is varied synchronously with each rising edge of the third dot clock signal DCKXX (FIG. 9(*e*)) after the horizontal synchronizing signal HSYNC2 (FIG. 9(*a*)) is returned to the high level. As discussed previously, an edge of the third dot clock signal DCKXX is delayed by a predetermined time period from an edge of the first dot clock signal DCK2. The latch timing in the first latch 154 thus does not overlap the timing of variation in count DC, so that the value of the horizontal address HADD is made stable.

As discussed above, the magnification MH2 in the horizontal direction and the magnification MV2 in the vertical direction can be set independently as shown in the bottom of FIG. 8, by adjusting the preset value N of the PLL circuit 142 and the preset value M of the frequency divider 144 shown in FIG. 6. A video image can be reproduced on the whole screen of the LCD panel 40 by setting the magnification MH2 in the horizontal direction equal to the ratio of [the horizontal resolution of the LCD panel 40] to [the horizontal resolution of the input video signal VPC] and by setting the magnification MV2 in the vertical direction equal to the ratio of [the vertical resolution of the LCD panel 40] to [the vertical resolution of the input video signal VPC].

FIG. 11 is a block diagram illustrating the structure of a down-converter as a second embodiment according to the present invention. The down-converter has a video signal selection unit 200 in addition to the input unit of the liquid-crystal projector shown in FIG. 1. The down-converter further includes a video encoder 202 in place of the LCD driver 38, and a variety of output devices (such as a television receiver 204, a video player 206, and a CD-RAM 208) in place of the LCD panel 40 and the light source 42.

The video signal selection unit 200 receives two television signals STV1 and STV2 as well as video signals (VPC, SYNC) generated by a personal computer, and selects one of the received signals. The television signals STV1 and STV2 are composite video signals including synchronizing signals.

When the video signal selection unit 200 selects a composite video signal, a decoder (not shown) in the video signal selection unit 200 generates component video signals VIN and a synchronizing signal SYNC from the selected composite video signal.

The video encoder 202 generates a composite video signals from a digital video signal DOUT and the reading-out synchronizing signals (DCK2, HSYNC2, and VSYNC2) output from the video scaler 36. The composite video signal thus generated is supplied to the television receiver 204 and the video player 206. In order to write a video image into the CD-RAM 208 (write-enable compact disk unit), the video encoder 202 does not generate a composite video signal but directly supplies the digital video signal DOUT and the reading-out synchronizing signals to the CD-RAM 208. The video scaler 36 can change the resolution of a video image to a desired resolution as discussed previously. When the user specifies a desired resolution, the video scaler 36 can output video images with the desired resolution corresponding to the various output devices. The apparatus of FIG. 11 is called down-converter because it can convert a variety of input video signals down to a variety of output video signals.

The present invention is not restricted to the above embodiments or applications. There may be many modifications, changes, and alterations without departing from the scope and spirit of the main characteristics of the inventions follows.

(1) The functions of the frequency determination unit 26 and the resolution determination unit 28 (see FIG. 1) realized by the computer program codes in the above embodiments may be realized by hardware circuits.

(2) In the above embodiments, image expansion and contraction are carried out when video images are read out from the frame memory 34. The image expansion and contraction may, however, be executed when video images are written into the frame memory 34.

(3) Any technique other than the frequency control discussed above may be applied to the image expansion and contraction. For example, they can be attained by multiplying the read address or the write address by a predetermined coefficient to change the addresses so that the image is expanded or contracted according to the changed addresses. FIGS. 12A and 12B1–12B3 show a process of expanding and contracting a video image by multiplying read address by a predetermined coefficient K. FIG. 12A shows a video image stored in the frame memory 34, whereas FIGS. 12B1 through 12B3 show expanded or contracted video images. In the drawing, Di,j represents video data written at an address (i,j) in the frame memory 34.

In the example of FIGS. 12A and 12B1–12B3, it is assumed that a memory resolution is defined by Mx (dots) by My (lines) and a display resolution Nx (dots) by Ny (lines). The coefficients K(Kx,Ky) by which the addresses are multiplied are given as follows:

$$Kx=Mx/Nx \tag{1a}$$

$$Ky=My/Ny \tag{1b}$$

A read address (XADD,YADD) used for reading out video data from the frame memory 34 is converted to a new read address (XADD,YADD) by the following equations:

$$XADD=INT(Kx\times XADD) \tag{2a}$$

$$YADD=INT(Ky\times YADD) \tag{2b}$$

wherein the operator INT( ) represents an operation of taking an integral portion of the value in parentheses.

FIG. 12B1 shows an example of the displayed image when the coefficients Kx and Ky are greater than 1.0 (for example, Kx=Ky=2.0). When the original horizontal address XADD is increased one by one, such as 0,1,2, . . . , the converted horizontal address XADD is varied as 0,2,4, . . . according to Equation (2a) given above. The vertical address YADD is converted in the same manner. Video data are read out from the frame memory 34 according to the converted read addresses XADD and YADD, so that a contracted video image is displayed as shown in FIG. 12B1. The horizontal magnification and the vertical magnification in this contracting process are respectively equal to 1/Kx and 1/Ky.

When the coefficients Kx and Ky are equal to 1.0, a video image in the frame memory 34 is displayed without any expansion or contraction as shown in FIG. 12B2.

FIG. 12B3 shows an example of the displayed image when the coefficients Kx and Ky are smaller than 1.0 (for example, Kx=Ky=0.7). When the original horizontal address XADD is increased one by one as 0,1,2,3, . . . , the converted horizontal address XADD is varied as 0,0,1,2, . . . The vertical address YADD is converted in the same manner. Video data are read out from the frame memory 34 according to the converted read addresses XADD and YADD, so that an expanded video image is displayed as shown in FIG. 12B3.

It is possible to set arbitrary values to Kx and Ky independently.

(4) When a high-speed read/write memory, such as a synchronous DRAM, is used for the frame memory 34, high-speed reading and writing of video signals can be carried out.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. A video image scaling apparatus for receiving a video image output as a video signal in a first format for a first display device and outputting the video image in a second format for a second display device, said apparatus comprising:

frequency determination means for analyzing the video signal to determine a frequency of synchronizing signals when the video signal is output in the first format;

image size determination means for determining an image size of the video signal by analyzing the frequency of the synchronizing signals of the video signal output in the first format; and

scaling means for scaling the video image expressed by the video signal in the first format by utilizing the synchronizing signals and the determined image size so that the video signal is output in the second format of said second display device.

2. A video image scaling apparatus in accordance with claim 1, wherein said image size determination means comprises:

image size storage means for storing relationships which identify the image size of the video signal in the first format based on the frequency of the synchronizing signals of the video signal; and

means for determining the image size of the video signal in the first format by referencing said image size storage means according to the frequency of the synchronizing signals of the video signal.

3. A video image scaling apparatus in accordance with claim 2, said apparatus further comprising:

means for displaying a sign indicating that an image size is unknown when the frequencies of the synchronizing signals of the video image are not stored in said image size storage means; and

image size setting means for setting a value of the unknown image size of the video signal and registering a relation between the image size and the frequencies of the synchronizing signals of the video signal in said image size storage means.

4. A video image scaling apparatus in accordance with claim 1, wherein said scaling means comprises:

a first buffer memory for temporarily storing the input video signal;

a frame memory in which a video signal read out of said first buffer memory is written;

a second buffer memory for temporarily storing a video signal read out of said frame memory; and

memory control means for giving a write address to said frame memory while successively reading out video signals from said first buffer memory to write the video signal read out of said first buffer memory into said frame memory, and for giving a read address to said frame memory to read out the video signal from said frame memory and transfer the video signal to said second buffer memory, and wherein

said memory control means comprises:

means for expanding or contracting a video image read out of said frame memory by adjusting the read address given to said frame memory.

5. A method for receiving a video image output as a video signal in a first format for a first display device and outputting the video image in a second format for a second display device, said method comprising the steps of:

(a) analyzing the video signal to determine a frequency of synchronizing signals when the video signal is output in the first format;

(b) determining an image size of the video signal by analyzing the frequency of the synchronizing signals of the video signal output in the first format; and

(c) scaling the video image expressed by the video signal in the first format by utilizing the synchronizing signals and the determined image size so that the video signal is output in the second format of said second display device.

6. A method in accordance with claim 5, wherein said step (b) comprises the steps of:

storing, in a memory, relationships which identify the image size of the video signal in the first format based on the frequency of the synchronizing signals of the video signal; and

determining the image size of the video signal in the first format by referencing said memory according to the frequency of the synchronizing signals of the video signal.

7. A method in accordance with claim 6, further comprising the steps of:

displaying a sign indicating that an image size is unknown when the frequencies of the synchronizing signals of the video image are not stored in said memory; and

setting a value of the unknown image size of the video signal and registering a relation between the image size and the frequencies of the synchronizing signals of the video signal in said memory.

8. A method in accordance with claim 5, wherein said step (b) comprises the steps of:

writing the input video signal into said frame memory; and

giving a read address to said frame memory to read out the video signal from said frame memory while adjusting the read address to expand or contract a video image read out of said frame memory.

9. A video image scaling apparatus for receiving a video image output as a video signal in a first format for a first display device and outputting the video image in a second format for a second display device, said apparatus comprising:

a video signal input for receiving a video signal, in the first format, including synchronizing signals;

a synchronizing signal frequency analyzer receiving the video signal from the video signal input and determining a frequency of the synchronizing signals when the video signal is output in the first format;

an image size determination unit for determining an image size of the video signal by analyzing the frequency of the synchronizing signals being applied to the video signal input; and

a scaling unit for scaling the video image expressed by the video signal in the first format by utilizing the synchronizing signals and the determined image size so that the video signal is output in the second format of said second display device.

10. A video image scaling apparatus in accordance with claim 9, wherein the image size determination unit comprises:

a memory unit for storing relationships which identify the image size of the video signal in the first format based on the frequency of the synchronizing signals of the video signal; and

a lookup unit for looking up frequencies in the memory unit to determine the image size of the video signal output in the first format.

11. A video image scaling apparatus in accordance with claim 10, further comprising:

an indicator for indicating that an image size is unknown when the frequency of the synchronizing signals are not stored in the memory unit; and

a memory unit updating unit for setting in the memory unit (1) a value of the unknown image size of the video signal and (2) a relation between the unknown image size and the frequency of the synchronizing signals.

12. A video image scaling apparatus in accordance with claim 9, wherein said scaling unit comprises:

a first buffer memory for temporarily storing the video signal;

a frame memory in which a video signal read out of said first buffer memory is written;

a second buffer memory for temporarily storing a video signal read out of said frame memory; and

a memory controller for applying a write address to said frame memory while successively reading out video signals from said first buffer memory to write the video signal read out of said first buffer memory into said frame memory, and for applying a read address to said frame memory to read out the video signal from said frame memory and transfer the video signal to said second buffer memory, and wherein

said memory controller includes a read address updating unit which expands or contracts a video image read out of said frame memory by adjusting a read address given to said frame memory.

* * * * *

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(12) **United States Patent**
Pether

(10) Patent No.: **US 6,741,263 B1**
(45) Date of Patent: **May 25, 2004**

(54) **VIDEO SAMPLING STRUCTURE CONVERSION IN BMME**

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(73) Assignee: **LSI Logic Corporation**, Milpitas, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 273 days.

(21) Appl. No.: **09/960,578**

(22) Filed: **Sep. 21, 2001**

(51) **Int. Cl.**[7] **G09G 5/02**
(52) **U.S. Cl.** **345/600**; 345/604; 348/453
(58) **Field of Search** 345/600, 601, 345/603, 604, 605, 690, 698; 348/441, 445, 446, 450, 453, 663, 665

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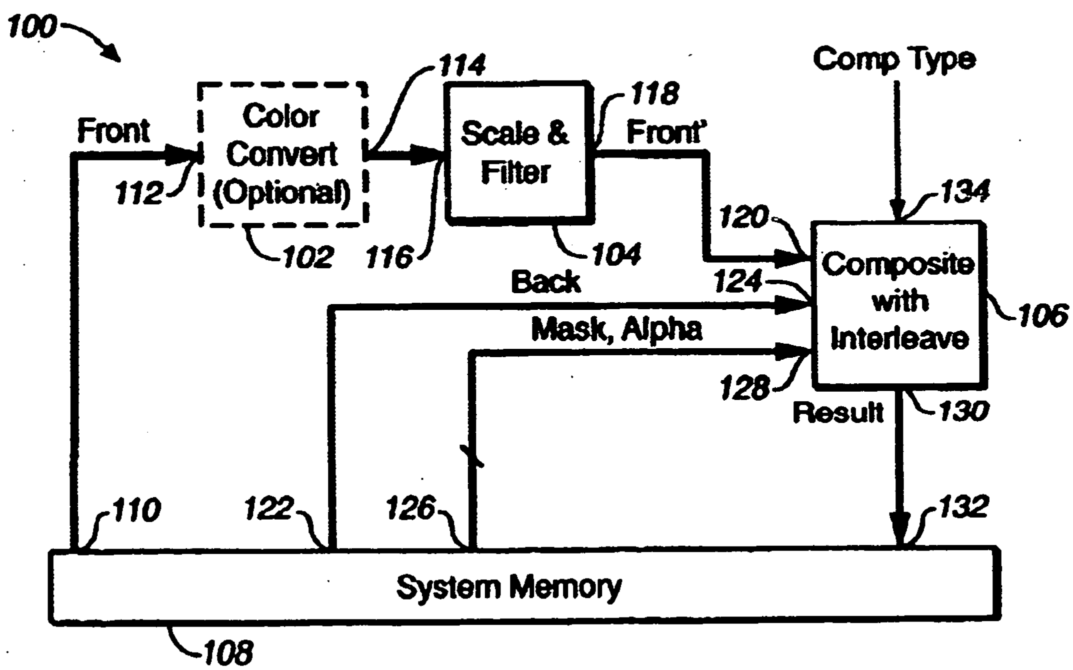
(57) **ABSTRACT**

An apparatus comprising a data modification circuit and a composite circuit. The data modification circuit may be configured to generate a first and second video component in response to a video data stream. The composite circuit may be configured to present an output graphics stream by interleaving the first and the second video component.

20 Claims, 5 Drawing Sheets



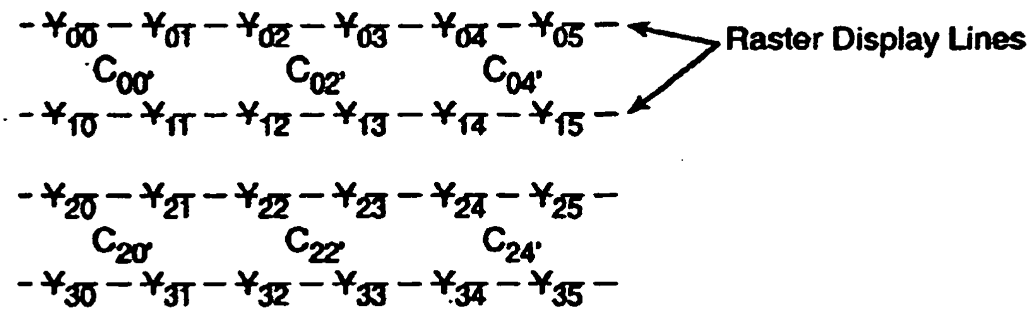


FIG._1

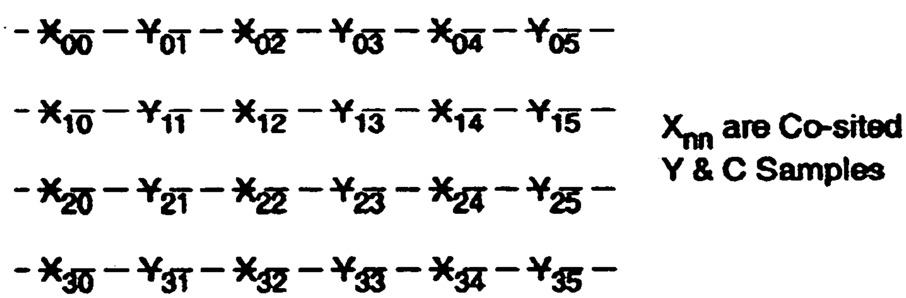


FIG._2

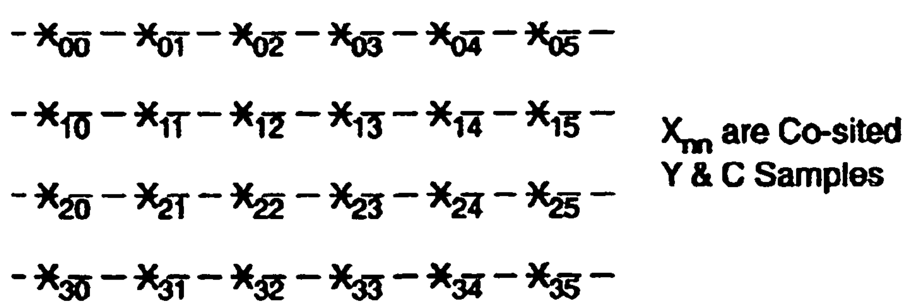


FIG._3

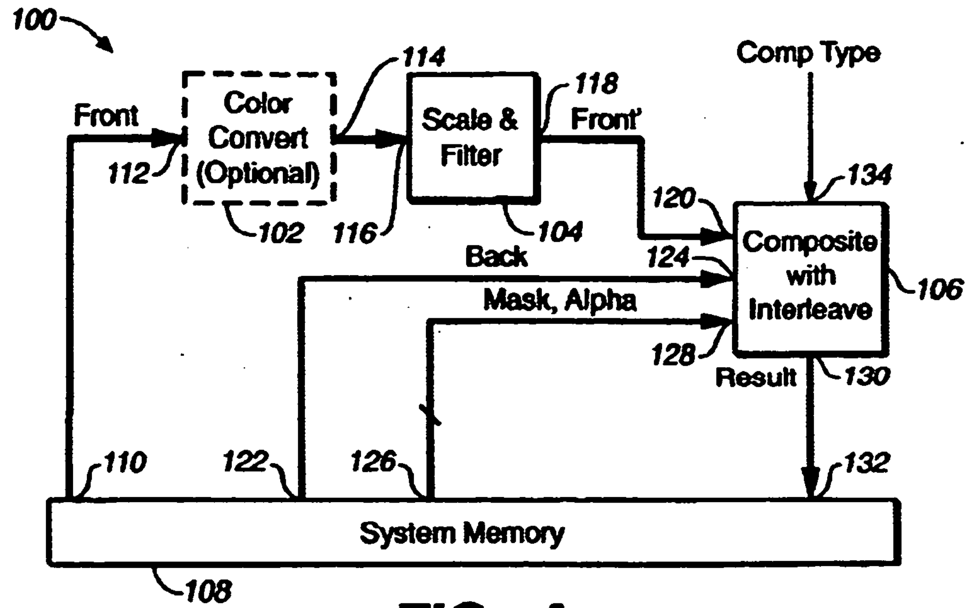

100
Front
Color
Convert
(Optional)
112
102
114
Scale &
Filter
116
104
118
Front'
Comp Type
134
120
124
Back
Composite
with
Interleave
106
Mask, Alpha
128
Result
130
110
122
126
132
System Memory
108

FIG._4

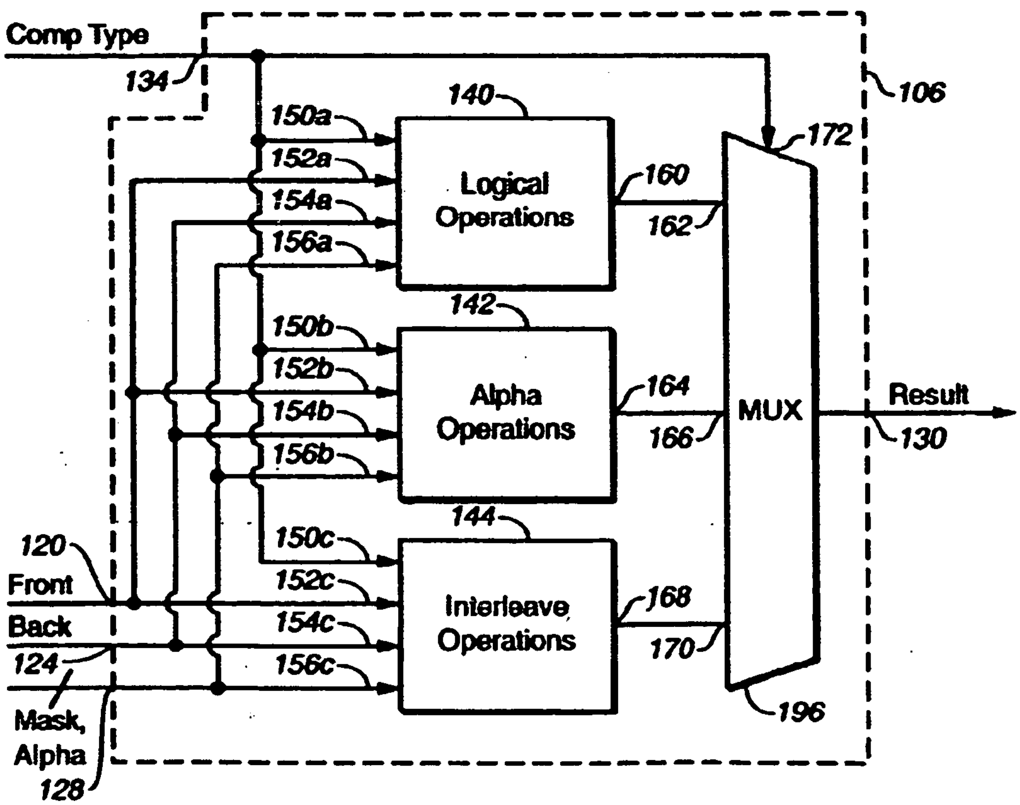

Comp Type
134
106
140
150a
152a
154a
156a
Logical
Operations
160
162
172
142
150b
152b
154b
156b
Alpha
Operations
164
166
MUX
Result
130
144
150c
152c
154c
156c
Interleave
Operations
168
170
196
120
Front
Back
124
Mask,
Alpha
128

FIG._5

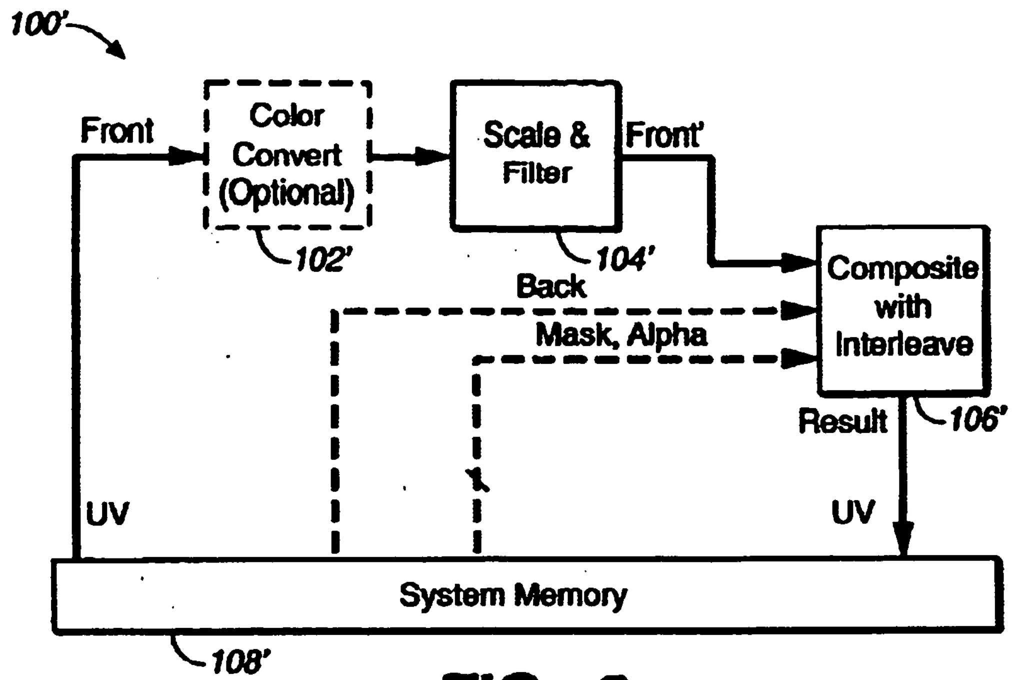

100'
Front
Color Convert (Optional)
Scale & Filter
Front'
102'
104'
Back
Composite with Interleave
Mask, Alpha
Result
106'
UV
UV
System Memory
108'

FIG._6

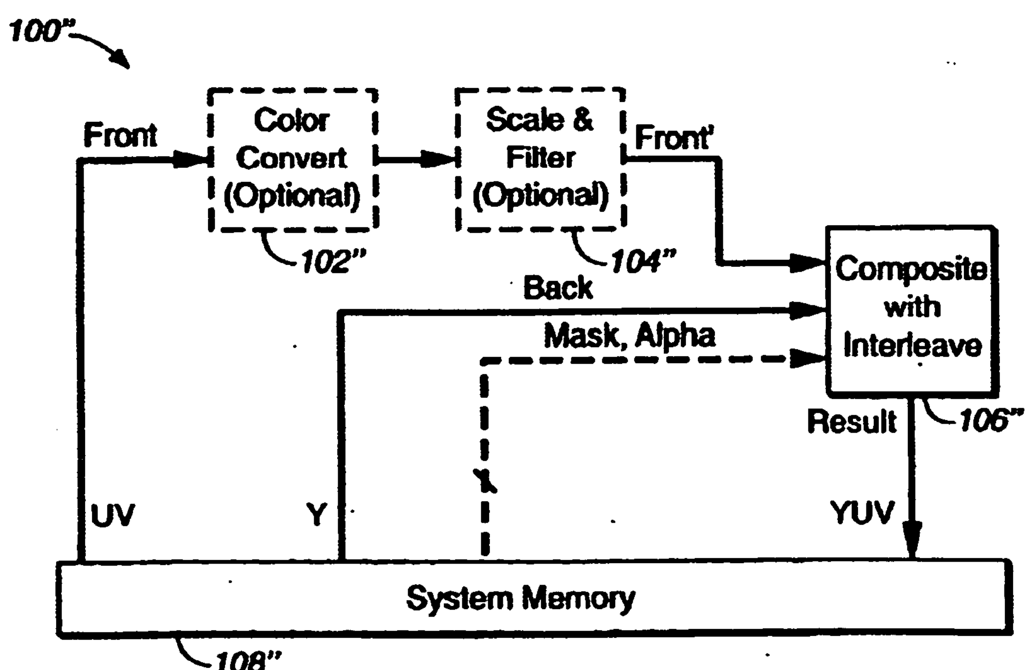

100"
Front
Color Convert (Optional)
Scale & Filter (Optional)
Front'
102"
104"
Back
Composite with Interleave
Mask, Alpha
Result
106"
UV
Y
YUV
System Memory
108"

FIG._7

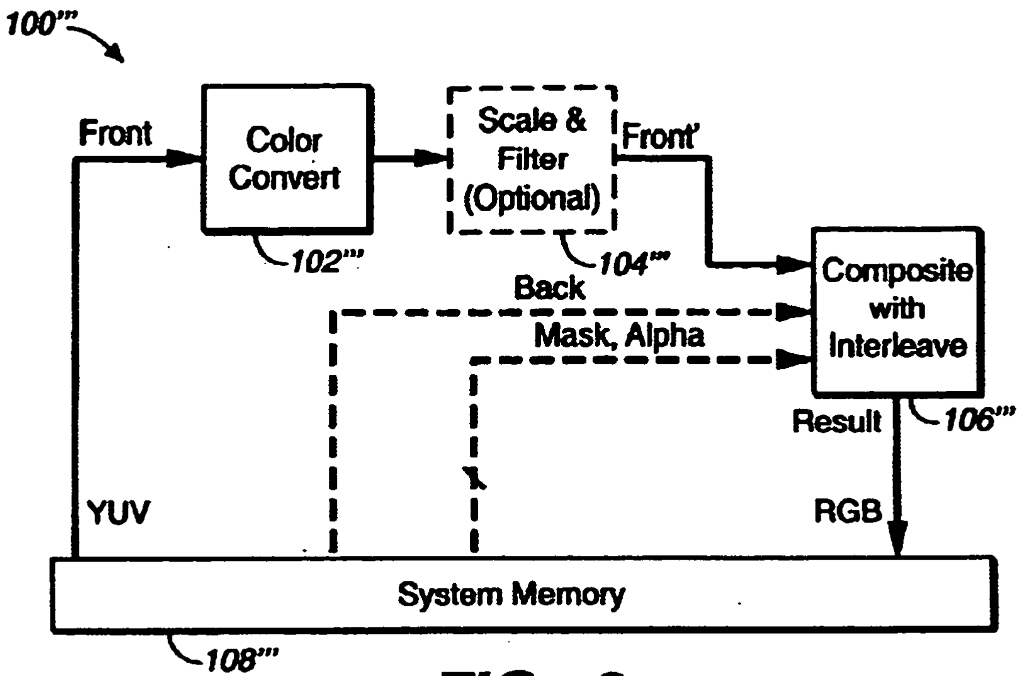

100'''
Front
Color Convert
Scale & Filter (Optional)
Front'
102'''
104'''
Back
Composite with Interleave
Mask, Alpha
Result
106'''
YUV
RGB
System Memory
108'''

FIG._8

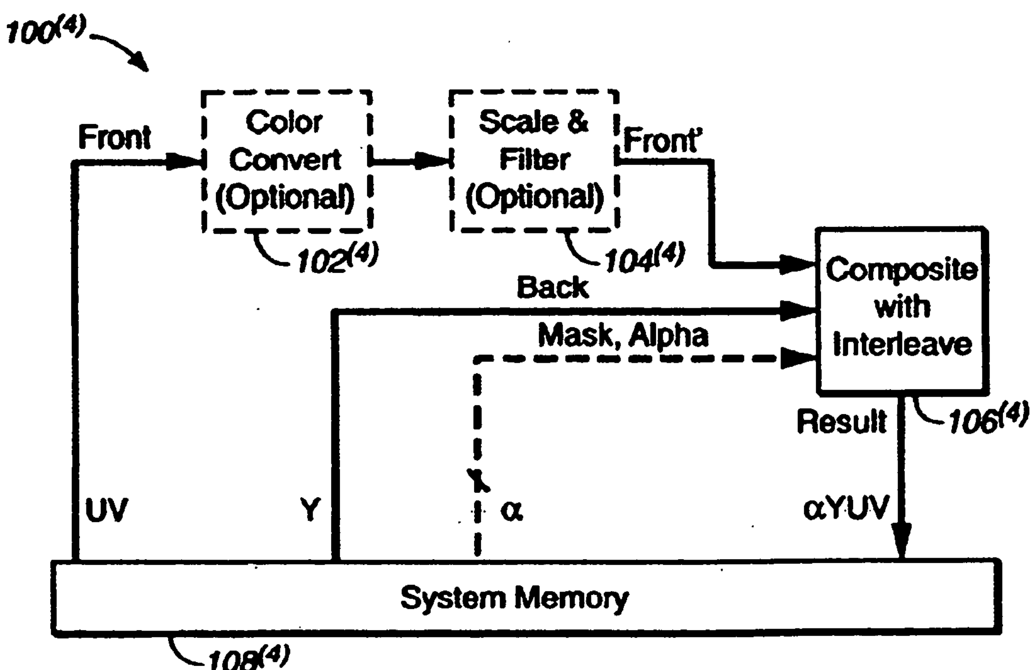
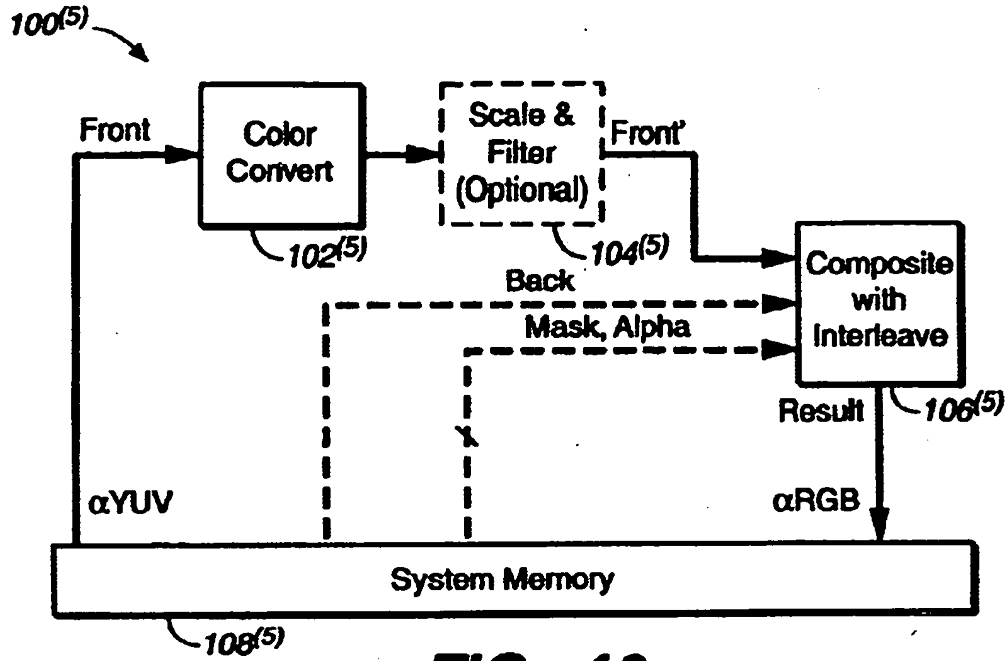
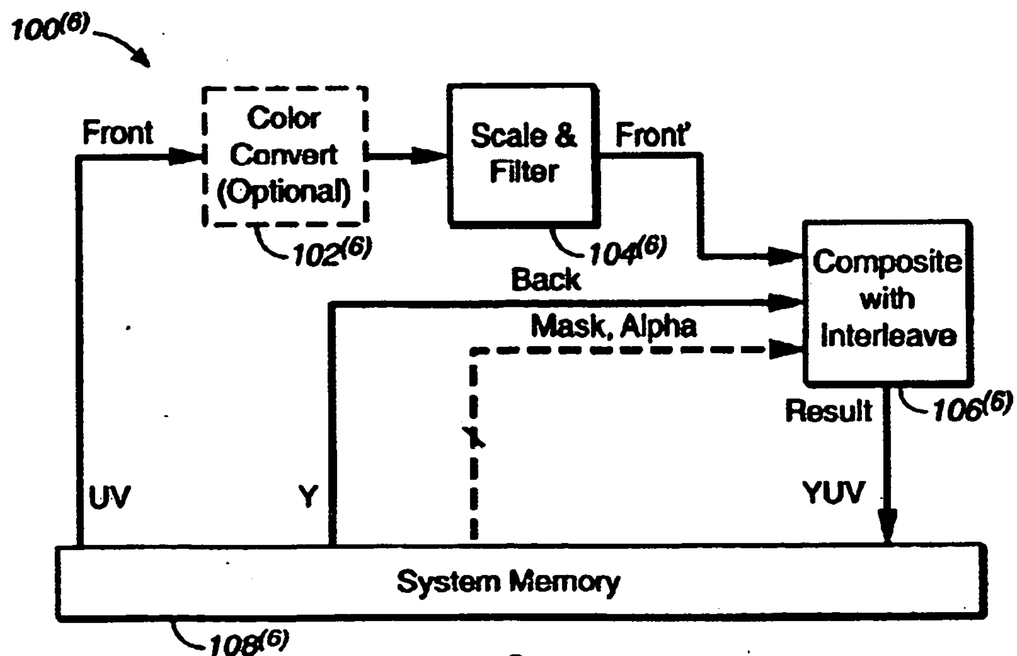

100(4)
Front
Color Convert (Optional)
Scale & Filter (Optional)
Front'
102(4)
104(4)
Back
Composite with Interleave
Mask, Alpha
Result
106(4)
UV
Y
α
αYUV
System Memory
108(4)

FIG._9



100(5)
Front
Color Convert
Scale & Filter (Optional)
Front'
102(5)
104(5)
Composite with Interleave
Back
Mask, Alpha
Result
106(5)
αYUV
αRGB
System Memory
108(5)

FIG._10



100(6)
Front
Color Convert (Optional)
Scale & Filter
Front'
102(6)
104(6)
Composite with Interleave
Back
Mask, Alpha
Result
106(6)
UV
Y
YUV
System Memory
108(6)

FIG._11

VIDEO SAMPLING STRUCTURE CONVERSION IN BMME

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application may relate to co-pending application Ser. No. 09/960,572, filed Sep. 21, 2001 and Ser. No. 09/878,594, filed Jun. 11, 2001, which are hereby incorporated by reference in their entirety.

FIELD OF THE INVENTION

The present invention relates to a method and/or architecture for integrating video and graphics processing in a single processor generally and, more particularly, to data modification used to allow changes in sampling structure for video to graphics data conversion.

BACKGROUND OF THE INVENTION

Digital video and/or graphics systems sample and store video in one of a number of formats, each of which include a Y and a C component (the Y component refers to a luminance component of the video and the C component refers to a chrominance component (i.e., a U, V pair)). For convenience with video formats, the Y data is normally stored as a block in one region of memory and the C data (the U, V pairs) is stored as a separate block. For simplicity, the present application will refer to all video and graphics components/samples as 8-bit quantities.

Referring to FIG. 1, a conventional video format 4:2:0 is shown. The video format 4:2:0 has one C sample (i.e., one U, V sample pair) for every group of four Y samples. The effective sample point for the C component is in a center of a square of Y components. In the 4:2:0 format of FIG. 1, an amount of Y component storage required (i.e., 4) is twice that required for the C component (i.e., 2), since each C component comprises a U and a V value.

Referring to FIG. 2, a conventional video format 4:2:2 is shown. The video format 4:2:2 has one U,V sample pair for every pair of Y samples. In the 4:2:2 format of FIG. 2, the C sampling point is coincident with every other Y sample point along a raster line. In the 4:2:2 format, the amount of Y component storage required is identical to that required for the C component.

Referring to FIG. 3, a conventional video format 4:4:4 is shown. The video format 4:4:4 has an identical sample structure for the Y, U and V components. In the 4:4:4 format of FIG. 3, the amount of C component storage required is twice that required for the Y component. The 4:4:4 sampling structure is identical to that used for YUV format graphics data (i.e., 24-bit-per-pixel YUV, or 32-bpp αYUV-8888).

Approaches for conversion between video formats change the number of chrominance samples C relative to the luminance samples Y. In particular, to convert video data to graphics data, the following operations are required, where all conversions use the video format 4:4:4 as a common conversion step (i.e., conversion from 4:2:0, 4:2:2 or 4:4:4 video format to 4:4:4 graphics data):

(i) scaling and filtering operations in both the horizontal and vertical directions are necessary for conversion from 4:2:0 to 4:4:4. Since none of the existing 4:2:0 chrominance C sampling points are aligned with the luminance Y points, it is necessary to interpolate a complete set of C values using either 0.75:0.25 or 0.25:0.75 coefficient pairs for the interpolation;

(ii) scaling and filtering operations in the horizontal direction only is necessary for conversion from 4:2:2 to 4:4:4. All "even" samples along the register line (counting the first sample as sample 0) already have an accurate U,V co-sited sample which can remain unchanged. For "odd" samples a new value must be calculated. The value can be calculated by interpolating horizontally between the neighboring two "even" sample values for U and V; or

(iii) interleaving of data is required to combine the separate Y and C data blocks into 24-bpp YUV pixels for conversion from 4:4:4 to graphics YUV. Conversion from 4:4:4 to graphics RGB is similar to conversion to graphics YUV, and followed by a color conversion step to change from YUV to RGB.

It is therefore generally desirable to provide a method and/or architecture capable of video/graphics sampling structure conversion.

SUMMARY OF THE INVENTION

The present invention concerns an apparatus comprising a data modification circuit and a composite circuit. The data modification circuit may be configured to generate a first and second video component in response to a video data stream. The composite circuit may be configured to present an output graphics stream by interleaving the first and the second video component.

The objects, features and advantages of the present invention include providing a method and/or architecture for implementing a video sampling structure conversion engine that may also permit interleaving of Y and C component video data into a single video data stream which may then be easily converted to a graphics data format.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a 4:2:0 video sampling structure;

FIG. 2 is a 4:2:2 video sampling structure;

FIG. 3 is a 4:4:4 video sampling structure;

FIG. 4 is a block diagram of a preferred embodiment of the present invention;

FIG. 5 is a detailed block diagram of a composite with interleave circuit of FIG. 4;

FIG. 6 is a block diagram illustrating an example operation of the present invention;

FIG. 7 is a block diagram illustrating an example operation of the present invention;

FIG. 8 is a block diagram illustrating an example operation of the present invention;

FIG. 9 is a block diagram illustrating an example operation of the present invention;

FIG. 10 is a block diagram illustrating an example operation of the present invention; and

FIG. 11 is a block diagram illustrating an example operation of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The implementation of a block move engine (BME) (a bit blitter or blitting engine) for rapidly copying blocks of graphics data from one location in memory to another is generally used for graphics processing. BMEs may be

extended to include two input data streams of identical size, which are combined by a logical composition operation and written back to memory as a single data block. The demand for improvements in graphics speed and resolution and the convergence of video and graphics applications onto common platforms has made it desirable to incorporate a wider selection of functions within the general structure of a BME. The present invention may be configured to allow alteration of the sampling structure of video chrominance C components, thus permitting the conversion between video and graphics data formats.

Referring to FIG. 4, a block diagram of a circuit **100** is shown in accordance with a preferred embodiment of the present invention. The circuit **100** may implement a block modify and move engine (BMME) that may provide a generic framework for integrating video and graphics processing. The circuit **100** generally comprises a circuit **102**, a circuit **104**, a circuit **106** and a memory **108**. The circuit **102** may be implemented as a color conversion circuit. In certain applications, the color conversion circuit **102** may be optional (to be discussed in connection with FIGS. **6**, **7**, **9** and **11**). The circuit **104** may be implemented as a scale and filter circuit. The circuit **106** may be implemented as a composite with interleave circuit. The memory **108** may be implemented as a system memory. The circuit **100** may comprise a modified version of a typical composite section (e.g., the composite and interleave circuit **106**) that may permit interleaving of Y and C component video data to a single graphics data stream. Additionally, the circuit **100** may allow other functional blocks to be included to provide unique features required by a particular application.

The memory **108** may have an output **110** that may present a signal (e.g., FRONT) to an input **112** of the color convert circuit **102**. The circuit **102** may have an output **114** connected to an input **116** of the scale and filter circuit **104**. The scale and filter circuit **104** may have an output **118** that may present a signal (e.g., FRONT') to an input **120** of the circuit **106**. The system memory **108** may also have an output **122** that may present a signal (e.g., BACK) to an input **124** of the circuit **106** and an output **126** that may present a number of signals (e.g., MASK and ALPHA) to an input **128** of the circuit **106**. The signals MASK and ALPHA may be presented together or individually. Additionally, each of the signals MASK and ALPHA may or may not be required for a particular implementation. The circuit **106** may have an output **130** that may present a signal (e.g., RESULT) to an input **132** of the system memory **108**.

The composite with interleave circuit **106** may also have an input **134** that may receive a signal (e.g., COMPTYPE). The signal COMPTYPE may be externally generated and written to a BMME control register by a CPU (both of which are not shown). The signal COMPTYPE may control the type of data combination operation carried out by the composite and interleave block **106**. The various signals of the present invention may be implemented as multi-bit or single bit signals or busses.

Referring to FIG. 5, a detailed block diagram of the composite with interleave circuit **106** is shown. The circuit **106** generally comprises a circuit **140**, a circuit **142**, a circuit **144** and a circuit **146**. The circuit **140** may be implemented as a logical operations circuit (block). The circuit **142** may be implemented as an alpha operations circuit (block). The circuit **144** may be implemented as an interleave operations circuit (block). The circuit **146** may be implemented as a multiplexer.

The circuit **140** may have an input **150***a* that may receive the signal COMPTYPE, an input **152***a* that may receive the signal FRONT, an input **154***a* that may receive the signal BACK and an input **156***a* that may receive the signals MASK and ALPHA. Similarly, the circuits **142** and **144** may have, respectively, inputs **150***b* and **150***c* that may receive the signal COMPTYPE, inputs **152***b* and **152***c* that may receive the signal FRONT, inputs **154***b* and **154***c* that may receive the signal BACK and inputs **156***b* and **156***c* that may receive the signals MASK and ALPHA.

The circuit **140** may have an output **160** connected to an input **162** of the multiplexer **146**. The circuit **142** may have an output **164** connected to an input **166** of the multiplexer **146**. The circuit **144** may have an output **168** connected to an input **170** of the multiplexer **146**. The multiplexer **146** may have an input **172** that may receive the signal COMPTYPE. The multiplexer **146** may present a signal received from the circuit **140**, the circuit **142** or the circuit **144** as the signal RESULT in response to the signal COMPTYPE.

In a preferred embodiment of the present invention, a data modification section of the BMME **100** may comprise one or both of the circuits **102** and **104**. For example, when conversion of video to graphics RGB is needed, the color conversion block **102** may be implemented. When the video format 4:4:4 is the only format used, the scale and filter block **104** may be omitted. A suitable design for the color conversion block **102** is described in co-pending application U.S. Ser. No. 09/878,594, filed Jun. 11, 2001, which is hereby incorporated by reference in its entirety. A suitable design for the scale and filter block **104** maybe described in co-pending application U.S. Ser. No. 09/960,572, filed Sep. 21, 2001 and/or Ser. No. 09/878,594, filed Jun. 11, 2001, which are hereby incorporated by reference in their entirety.

The logical operations block **140** of the composite with interleave block **106** may implement logical bitwise operations such as:

RESULT=FRONT XOR BACK

RESULT=(MASK AND FRONT) OR ((NOT MASK) AND BACK).

The alpha operations block **142** of the composite with interleave circuit **106** may perform alpha-blending equations such as:

RESULT=(ALPHA*FRONT)+((1-ALPHA)*BACK)).

The interleave operations block **144** of the composite with interleave circuit **106** generally comprises multiplexers and bit shifters (not shown). The interleave operations block **144** may perform (but is not limited to) the following operations:

(i) take data from the bus FRONT and pass the data unchanged to the bus RESULT, (the data may be chroma (U,V) pairs, or YUV, RGB, αYUV or αRGB pixels);

(ii) take chroma-only (U,V) data from the bus FRONT and Y data from the bus BACK and combine the data to make up 24-bpp YUV values on the bus RESULT; and/or

(iii) take chroma-only (U,V) data from the bus FRONT, Y data from the bus BACK and alpha data from the bus ALPHA and combine the data to make up 32-bpp αYUV values on the bus RESULT.

Example operations of the interleave operations block **144** are shown in the following TABLES 1*a* and 1*b*.

TABLE 1a

	Front				Back			
Conversion	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0
4:2:0 to 4:4:4	U	V	U	V	—	—	—	—
4:2:2 to 4:4:4	U	V	U	V	—	—	—	—
4:4:4 to YUV	—	—	U	V	—	—	—	Y
4:4:4 to RGB	—	R	G	B	—	—	—	—
4:4:4 + alpha to αYUV	—	—	U	V	—	—	—	Y
αYUV to αRGB	A	R	G	B	—	—	—	—

TABLE 1b

	Mask/Alpha				Result			
Conversion	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0
4:2:0 to 4:4:4	—	—	—	—	U	V	U	V
4:2:2 to 4:4:4	—	—	—	—	U	V	U	V
4:4:4 to YUV	—	—	—	—	—	Y	U	V
4:4:4 to RGB	—	—	—	—	—	R	G	B
4:4:4 + alpha to αYUV	—	—	—	A	A	Y	U	V
αYUV to αRGB	—	—	—	—	A	R	G	B

The entries in the TABLE 1a and the TABLE 1b may relate to the conversion operations of the interleave circuit **144** of the composite with interleave circuit **106** (described in connection with FIGS. **6–11**). Input and output busses (e.g., the bus FRONT, the bus BACK, the bus MASK/ALPHA and an output interleave bus RESULT) may be 32-bits wide. Any color or alpha component bus (e.g., RGB or alpha) may be 8-bits wide. However, other appropriate bit widths may be implemented to meet the criteria of a particular implementation. Additionally, some input bits may not be used in one or more conversion operations. Such unused bits may be omitted when applicable.

Referring to FIGS. **6–11**, a variety of particular video data to graphics data conversion operations using circuits similar to the circuit **100** of FIG. **4**. are shown. Referring to FIG. **6**, a circuit **100'** is shown illustrating a 4:2:0 to 4:4:4 conversion. The circuit **100'** may be similar to the circuit **100**. To achieve the necessary conversion steps for producing graphics format data from video, the BMME **100'** may: (i) scale and filter in both the horizontal and vertical directions on chrominance data (the data may be required to be passed through the BMME **100'** twice, once for each filtering direction), (ii) interpolate a complete set of new chrominance C values, since the existing 4:2:0 chrominance C sampling points are not aligned with the luminance Y points, (iii) alternately set the filter coefficients to 0.75:0.25 and 0.25:0.75, and (iv) pass the scaled and filtered U, V samples through the composite with interleave block **106'** back to the bus RESULT unchanged. The color conversion circuit **102'** may not be used.

The BMME **100'** (e.g., video 4:2:0 to graphics 4:4:4 conversion) configuration may also be implemented for conversion of video 4:2:2 to graphics 4:4:4. However, a single scaling and filtering operation of chrominance C data may be performed in the horizontal direction only and the filter coefficients may be set to alternate between 1:0 and 0.5:0.5 in order to interpolate a new chrominance U,V pair between each existing U, V sample. The color conversion circuit **102'** is generally not used.

Referring to FIG. **7**, a circuit **100"** is shown illustrating a graphics 4:4:4 to graphics YUV conversion. The circuit **100"** may be similar to the circuit **100**. Interleaving of data may be performed to combine the separate Y and C data blocks into 24-bpp YUV pixels. The chrominance U, V values are generally input on the bus FRONT and the luminance Y value may be input on the bus BACK. The composite with interleave block **106"** may be set (configured) to perform the interleaving operation such that the YUV pixels are placed on the bus RESULT. The color conversion circuit **102** and the scaling and filter circuit **104** are generally not used.

Referring to FIG. **8**, a circuit **100'"** is shown illustrating a graphics 4:4:4 to graphics RGB conversion. The circuit **100'"** may be similar to the circuit **100**. For conversion of graphics 4:4:4 to graphics RGB, a first step may be similar to the graphics 4:4:4 to graphics YUV conversion. A second step may be a color conversion process, where the YUV data on the bus FRONT may be converted to RGB format and passed directly to the bus RESULT.

Referring to FIG. **9**, a circuit $\mathbf{100^{(4)}}$ is shown illustrating a graphics 4:4:4 and alpha to graphics αYUV conversion. The circuit $\mathbf{100^{(4)}}$ may be implemented similarly to the circuit **100**.

Referring to FIG. **10**, a circuit $\mathbf{100^{(5)}}$ is shown illustrating a graphics αYUV to graphics αRGB conversion. The circuit $\mathbf{100^{(5)}}$ may be similar to the circuit **100**. The present invention may also include alpha components. The circuit $\mathbf{100^{(4)}}$ or the circuit $\mathbf{100^{(5)}}$ may include any interleaving and/or color conversion process of an alpha channel value.

Referring to FIG. **11**, a circuit $\mathbf{100^{(6)}}$ is shown illustrating a 4:2:2 to graphics YUV conversion. The circuit $\mathbf{100^{(6)}}$ may be similar to the circuit **100**. The circuit $\mathbf{100^{(6)}}$ may combine filtering and interleaving within a single circuit. The circuit $\mathbf{100^{(6)}}$ may reduce the 4:2:2 to graphics YUV operation to a single pass of data through the BMME $\mathbf{100^{(6)}}$. Such a configuration may provide a savings in processing time and system bus usage. In the case of 4:2:0 to graphics YUV, the second filtering pass may be combined with the interleaving operation.

The present invention may provide a video sampling structure conversion engine that may permit interleaving of luminance and chrominance video data into a single video data stream. The single video data stream may be easily converted to a graphics data format.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An apparatus comprising:

a memory connected to a first input bus, a second input bus and an output bus;

a converter circuit configured to generate a first intermediate signal in response to converting a color format for a first data stream received on said first input bus;

a scale and filter circuit configured to generate a second intermediate signal by scaling and filtering said first intermediate signal; and

a composite circuit configured to generate an output graphics stream on said output bus by interleaving said second intermediate signal and a second data stream received on said second input bus.

2. The apparatus according to claim **1**, wherein said apparatus comprises a block modify and move engine (BMME) configured to modify a plurality of blocks from said first data stream while moving said blocks from one location to another location in said memory.

3. The apparatus according to claim 1, wherein said apparatus comprises a video sampling conversion block modify and move engine.

4. The apparatus according to claim 1, wherein said apparatus is configured to permit conversion between video data and graphics data.

5. The apparatus according to claim 1, wherein said composite circuit comprises:

a logical operations circuit configured to perform logical bitwise operations on said first data stream and said second data stream;

a alpha operations circuit configured to perform alpha-blending between said first data stream and said second data stream; and

an interleave operations circuit configured to perform one or more predetermined interleave operations using said first data stream.

6. The apparatus according to claim 5, wherein said one or more predetermined interleave operations are selected from the group consisting of (i) receive data from said first input bus and pass said data unchanged to said output bus, (ii) receive chrominance data from said first input bus and luminance data from said second input bus and combine said chrominance and said luminance data to form a first particular output value on said output bus, and (iii) receive said chrominance data from said first input bus, said luminance data from said second input bus and alpha data from a third input bus and combine said chrominance, said luminance and said alpha data to form a second predetermined value on said output bus.

7. The apparatus according to claim 1, further comprising:

a memory configured to interface to said composite circuit via a third input bus.

8. The apparatus according to claim 1, wherein said apparatus is configured to perform conversion of one or more video data formats to graphics data.

9. The apparatus according to claim 1, further comprising a third input bus disposed between said memory and said composite circuit to carry a mask signal to control masking of said first data stream.

10. The apparatus according to claim 1, further comprising a third input bus disposed between said memory and said composite circuit to carry an alpha signal to control an alpha-blending of said first data stream with said second data stream.

11. The apparatus according to claim 5, wherein said composite circuit is further configured to select one of said logical operations circuit, said alpha circuit and said interleave operations circuit to generate said output graphics stream in response to a command signal.

12. An apparatus comprising:

means for generating a first intermediate signal by modifying a color format for a first data steam received from a memory;

means for generating a second intermediate signal by scaling and filtering said first intermediate signal;

means for interleaving said second intermediate signal and a second data stream received from said memory to generate an output graphics stream; and

means for storing said output graphics stream in said memory.

13. A method for permitting conversion between video data and graphics data, comprising the steps of:

(A) generating a first intermediate signal by modifying a color format for a first data steam received from a memory;

(B) generating a second intermediate signal by scaling and filtering said first intermediate signal;

(C) interleaving said second intermediate signal and a second data stream received from said memory to generate an output graphics stream and;

(D) storing said output graphics stream in said memory.

14. The method according to claim 13; wherein step (C) comprises the sub-steps of:

(C-1) performing logical bitwise operations on said first data stream and said second data stream;

(C-2) performing alpha-blending between said first data stream and said second data stream; and

(C-3) performing one or more predetermined interleave operations using said first data stream.

15. The method according to claim 14, wherein sub-step (C-3) comprises one or more of the following steps:

(i) receiving data from a first input bus and passing said data unchanged to an output bus;

(ii) receiving chrominance data from said first input bus and luminance data from a second input bus and combining said chrominance and said luminance data to form a first particular output value on said output bus; and

(iii) receiving said chrominance data from said first input bus, said luminance data from said second input bus and alpha data from a third input bus and combining said chrominance, said luminance and said alpha data to form a second predetermined value on said output bus.

16. The method according to claim 15, further comprising the step of:

interfacing said memory with said first input bus and said output bus.

17. The method according to claim 13, further comprising the step of:

converting one or more video data formats in said first data stream to graphics data in said output graphics stream.

18. The method according to claim 13, wherein step (B) comprises the sub-step of filtering said first data stream in a first direction and said method further comprises the step of:

filtering said output graphics stream in a second direction.

19. The method according to claim 13, wherein step (C) comprises the sub-step of:

generating said output graphics stream by performing an exclusive OR operation between said first data stream and said second data stream.

20. The method according to claim 13, wherein step (C) comprises the sub-step of:

generating said output graphics stream by performing a masking operation on said first data stream and said second data stream.

* * * * *

US006128539A

United States Patent [19]

Markandey et al.

[11] Patent Number: 6,128,539

[45] Date of Patent: Oct. 3, 2000

[54] **METHOD AND APPARATUS FOR FORMING IMAGE SCALING FILTERS**

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[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **08/298,547**

[22] Filed: **Aug. 30, 1994**

[51] **Int. Cl.**[7] **G05B 13/02**; G06F 15/00

[52] **U.S. Cl.** **700/29**; 702/190

[58] **Field of Search** 364/488, 514, 364/572; 700/29; 702/190

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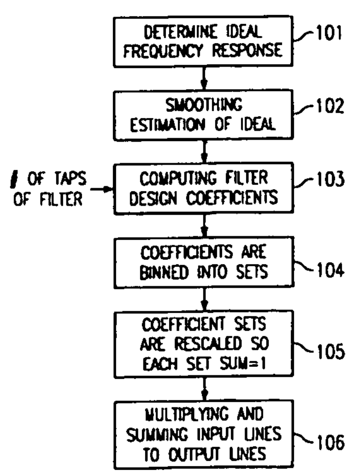
Primary Examiner—William A. Cuchlinski, Jr.
Attorney, Agent, or Firm—Robert L. Troike; Frederick J. Telecky, Jr.

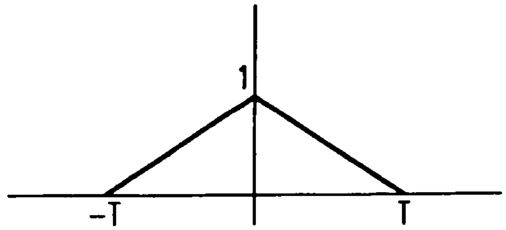
[57] **ABSTRACT**

A method of forming an image scaling filter for converting a first number of input lines to a second number of output lines comprises the steps of determining an optimal frequency response without sharp cutoffs for a given scaling factor and for a determined number of taps per line **102**. Filter coefficients are provided based on the determined filter taps per line and the determined optimal frequency response **103**. The coefficients are grouped into sets **104** corresponding to the taps per output line and the coefficients are rescaled so the sum of the set equals one **105**. The input lines are multiplied by the rescaled coefficients and summed **106** to achieve the output line values.

4 Claims, 8 Drawing Sheets



LINEAR INTERPOLATION FILTER:



FILTER KERNEL

FIG. 1a

ALIASING (3 TO 4 SCALING):

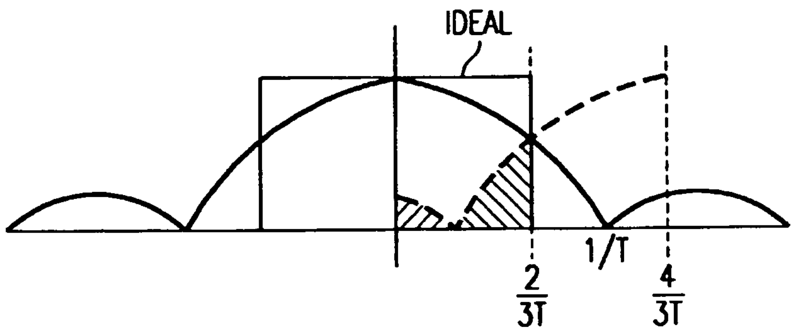
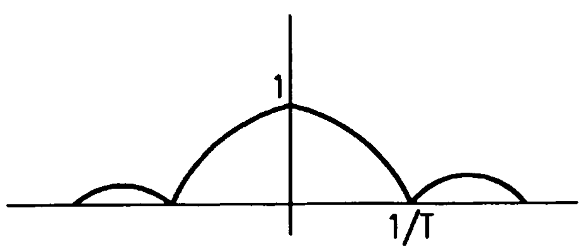


FIG. 1b



FREQUENCY RESPONSE

FIG. 1c

APERTURE EFFECT:

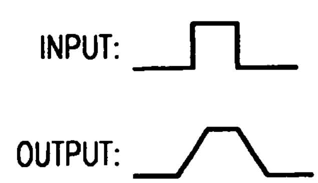


FIG. 1d

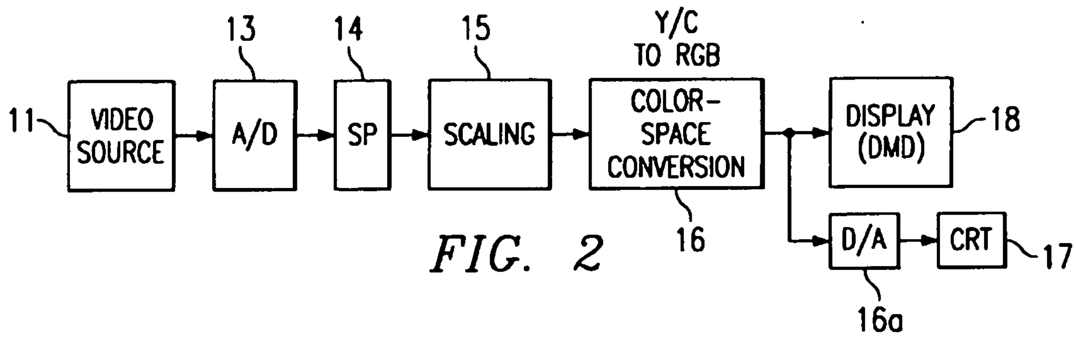

13
14
15
Y/C TO RGB
11
VIDEO SOURCE
A/D
SP
SCALING
COLOR-SPACE CONVERSION
DISPLAY (DMD)
18
16
D/A
CRT
17
16a

FIG. 2

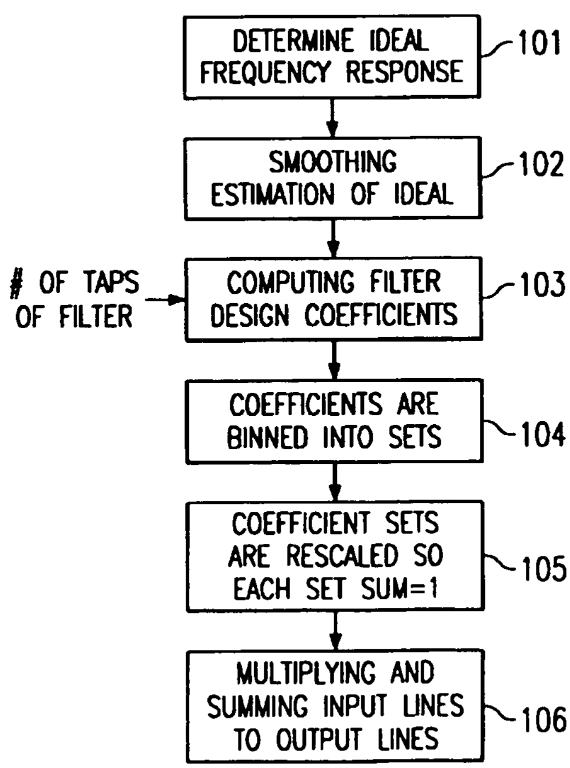

DETERMINE IDEAL FREQUENCY RESPONSE
101
SMOOTHING ESTIMATION OF IDEAL
102
OF TAPS OF FILTER
COMPUTING FILTER DESIGN COEFFICIENTS
103
COEFFICIENTS ARE BINNED INTO SETS
104
COEFFICIENT SETS ARE RESCALED SO EACH SET SUM=1
105
MULTIPLYING AND SUMMING INPUT LINES TO OUTPUT LINES
106

FIG. 3

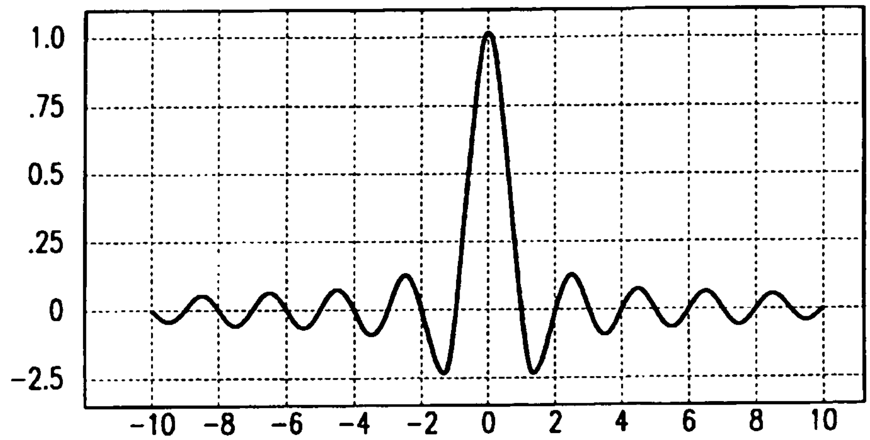
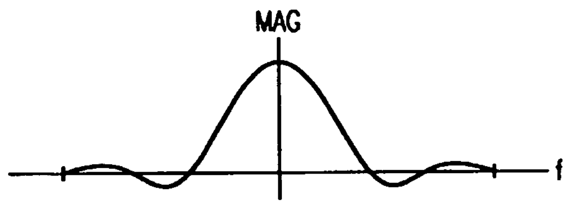


FIG. 4a



OPTIMAL FREQUENCY RESPONSE

FIG. 4b

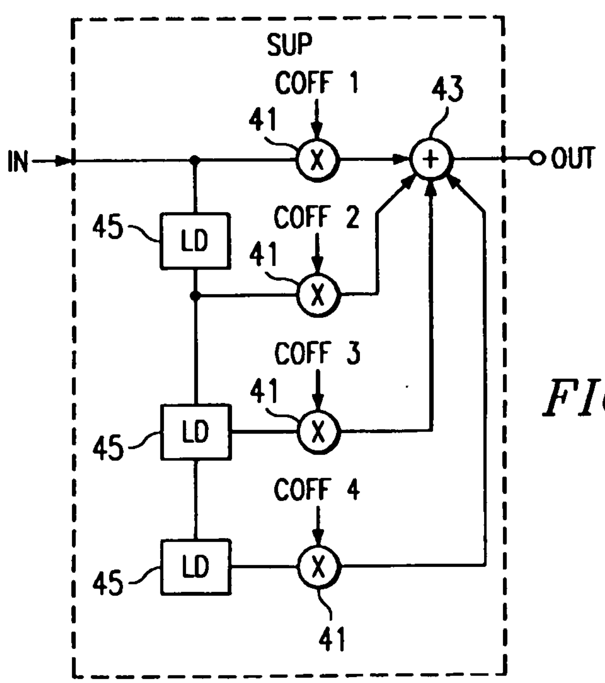


FIG. 5

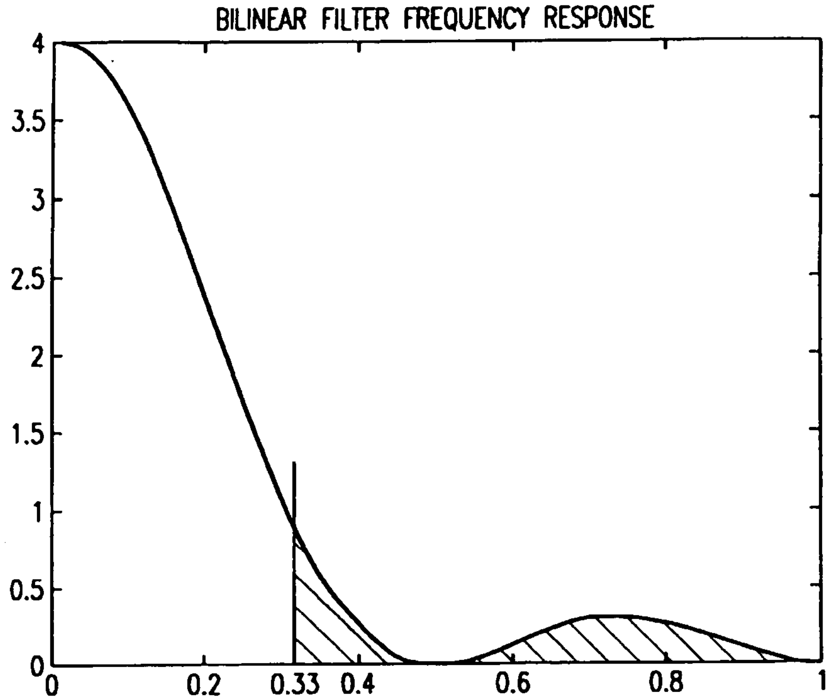

BILINEAR FILTER FREQUENCY RESPONSE
4
3.5
3
2.5
2
1.5
1
0.5
0
0
0.2
0.33
0.4
0.6
0.8
1

FIG. 6a

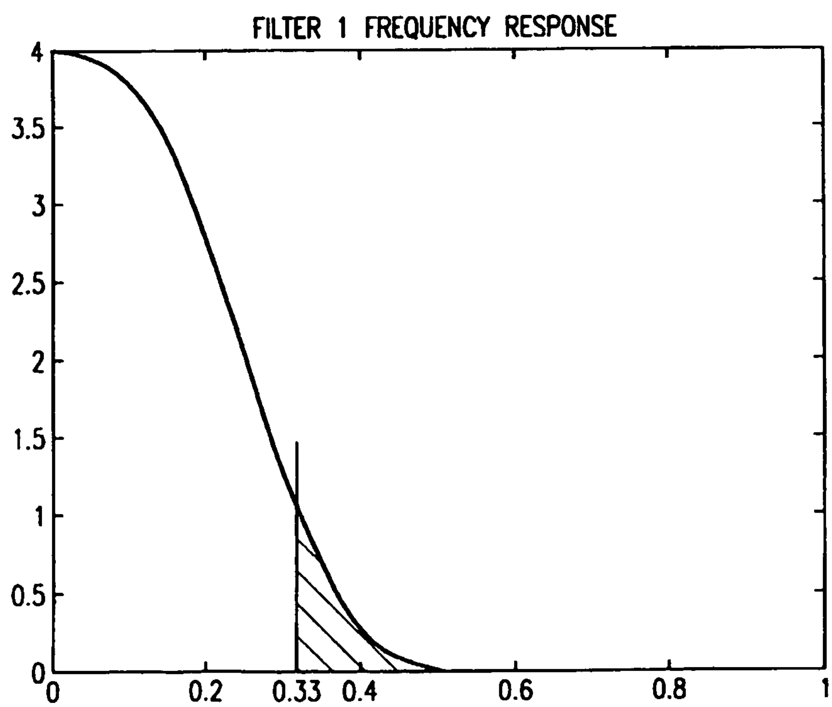

FILTER 1 FREQUENCY RESPONSE
4
3.5
3
2.5
2
1.5
1
0.5
0
0
0.2
0.33
0.4
0.6
0.8
1

FIG. 6b

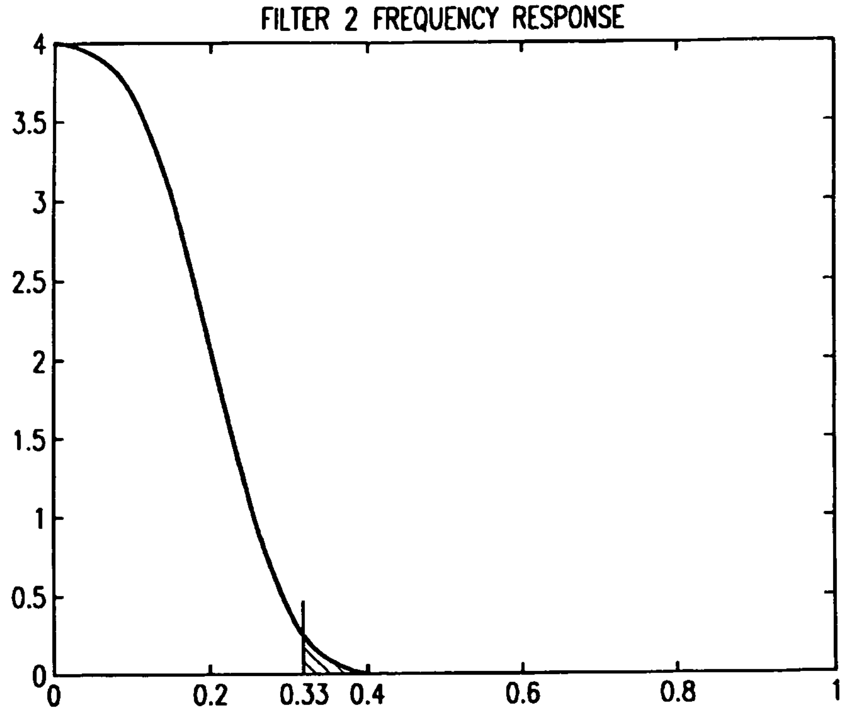

FILTER 2 FREQUENCY RESPONSE
4
3.5
3
2.5
2
1.5
1
0.5
0
0
0.2
0.33
0.4
0.6
0.8
1

FIG. 6c

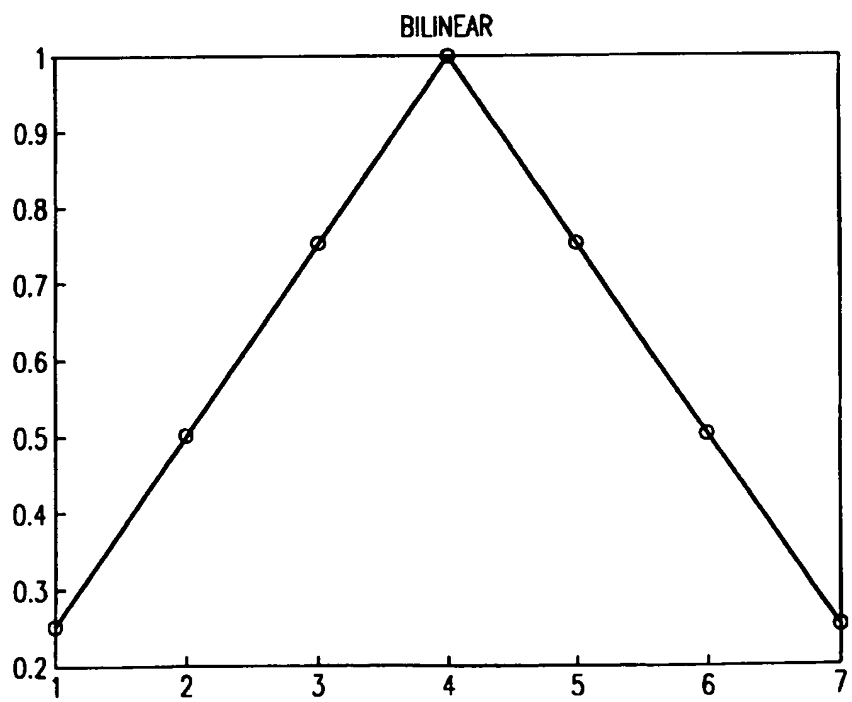

BILINEAR
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
1
2
3
4
5
6
7

FIG. 7a

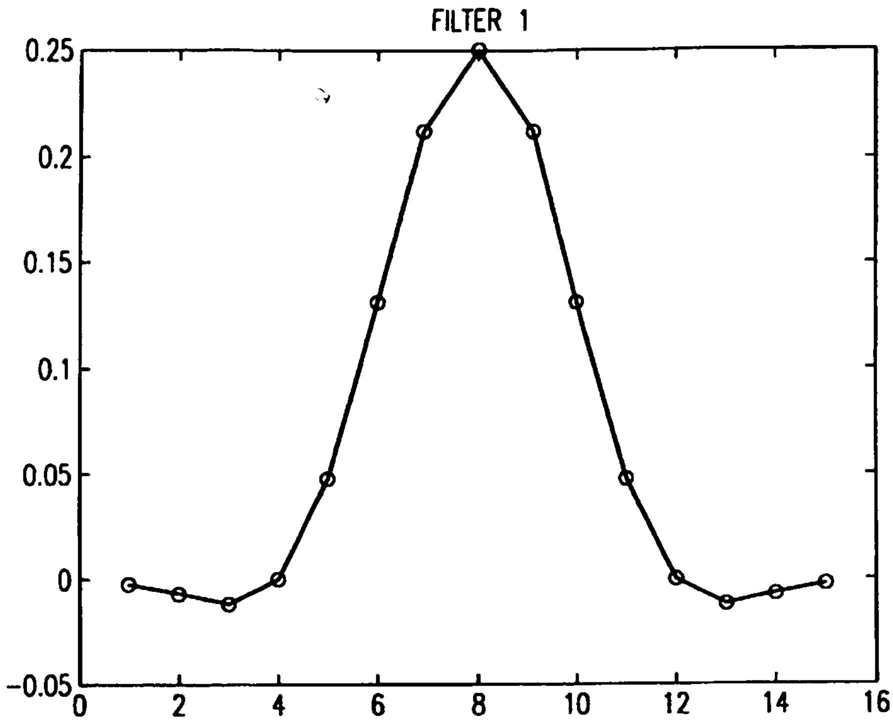

FILTER 1
0.25
0.2
0.15
0.1
0.05
0
−0.05
0
2
4
6
8
10
12
14
16

FIG. 7b

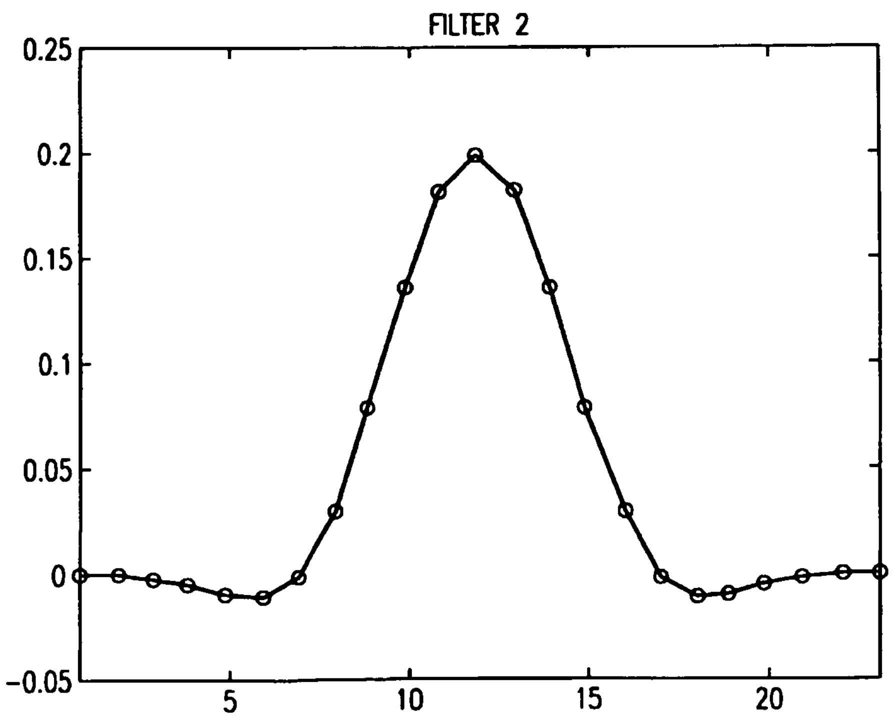

FILTER 2
0.25
0.2
0.15
0.1
0.05
0
−0.05
5
10
15
20

FIG. 7c

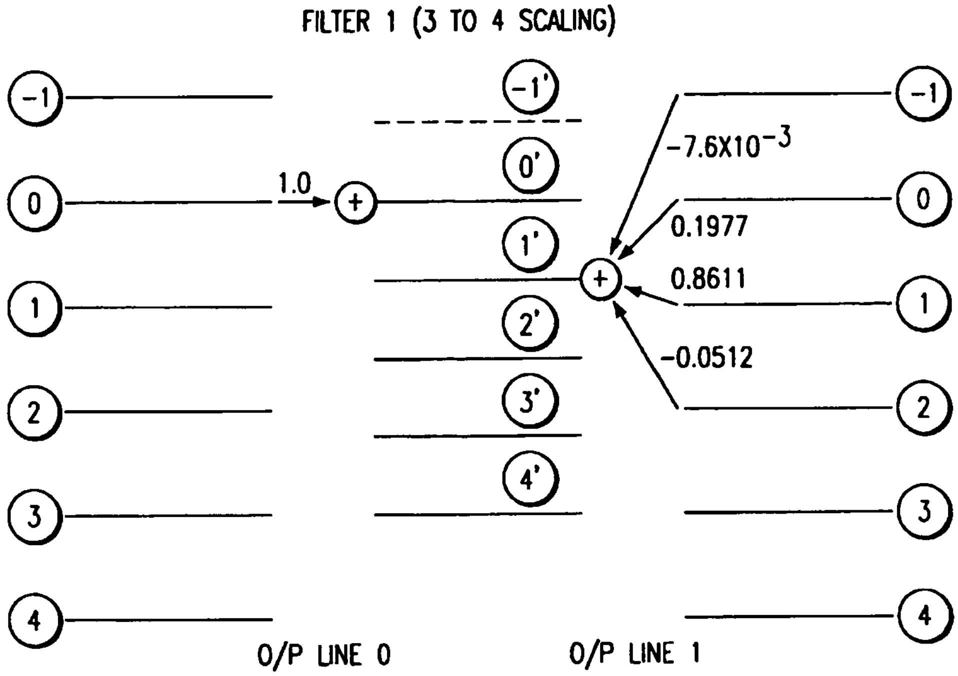

FILTER 1 (3 TO 4 SCALING)
-1
0
1
2
3
4
1.0
+
-1'
0'
1'
2'
3'
4'
-7.6X10^-3
0.1977
0.8611
-0.0512
O/P LINE 0
O/P LINE 1

FIG. 8a

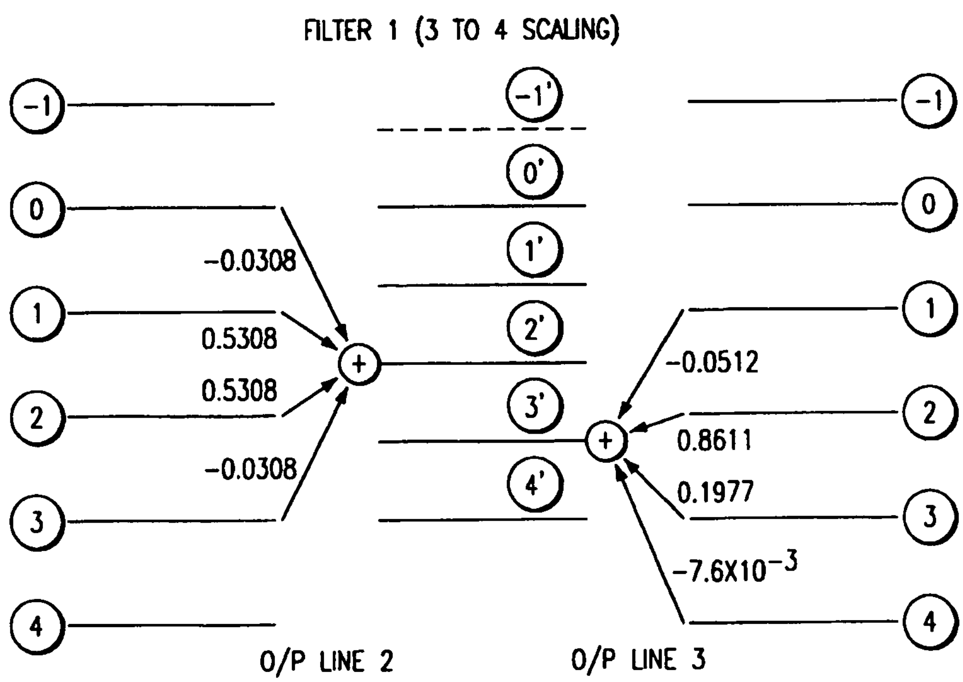

FILTER 1 (3 TO 4 SCALING)
-1
0
1
2
3
4
-0.0308
0.5308
0.5308
-0.0308
+
-1'
0'
1'
2'
3'
4'
-0.0512
0.8611
0.1977
-7.6X10^-3
O/P LINE 2
O/P LINE 3

FIG. 8b

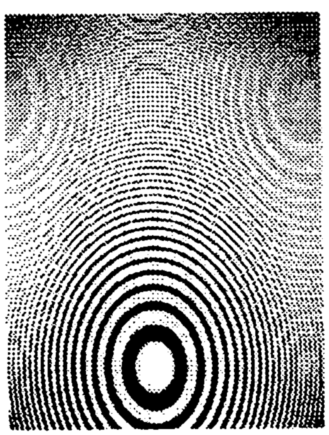


FIG. 9a

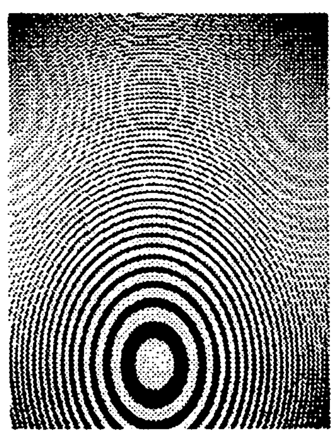


FIG. 9b

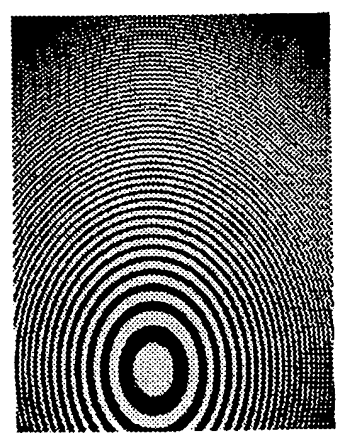


FIG. 9c

METHOD AND APPARATUS FOR FORMING IMAGE SCALING FILTERS

TECHNICAL FIELD OF THE INVENTION

This invention relates to displays and, more particularly, to the formation of image scaling filters for displays.

BACKGROUND OF THE INVENTION

It has become highly desirable to provide video displays in many formats. There are different modes for different image formats such as panoramic wide screen or movie. There are also different video formats for computer video displays depending upon whether the video display is a VGA (640 pixels in each row×480 rows of pixels, where a pixel is a picture element), or a super VGA, or an XGA, Further, there are different television formats from the standard NTSC to as much as 1920 pixels in each row by 1080 rows for High Definition TV (HDTV) format. Further there are flat panel displays and a Digital Mirror Device (DMD), which is a new projection display that utilize reflections from hundreds of thousands of micromirrors, each mounted above its own cell memory.

Within the operation of such a system, it may be desirable to have a panoramic view or wide screen view, or a movie screen view, again requiring some modifications of the number of lines of the video signal from a source to the number of lines in the output signal.

This is achieved by some form of image scaling. In order to achieve these changes in formats, scaling filters have been used. One such known filter is a bilinear interpolation filter, which suffers from the two problems of aliasing (unwanted patterns) and aperture effect, or image softening (blurring). These problems are illustrated in FIG. 1. FIG. 1*a* illustrates the bilinear filter kernel, FIGS. 1*b* and 1*c* illustrate the frequency response.

The aliasing problem can be understood by considering the frequency response of the bilinear filter for an example of a three to four scaling in FIG. 1. Image scaling is basically an image filtering and resampling operation. If X(w) is the frequency domain representation of the original signal, then the resampling operation will create a scaled image whose frequency domain representation contains shifted replicas of X(w), located at the new sampling frequency. These replicas can interact with each other if they are not completely separated from each other, leading to aliasing, as shown in the hatched portion in FIG. 1*b*.

The second problem is the aperture effect or image softening. This is caused by the fact that interpolation filters are basically low pass filters with high frequency roll-off as illustrated by the frequency response of bilinear interpolation in FIG. 1*d*.

Both of these problems relate to the frequency content of the signals and can become particularly objectionable with high bandwidth sources.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, an improved image scaling filter is achieved by estimating a close to ideal frequency response of the filter without sharp cut-offs. The estimated frequency response is then fed to a design algorithm along with the constraints such as a number of filters taps required, which computes a set of filter coefficients for scaling. The set of filter coefficients are scaled so that each set sums to a value of one. The appropriate set of input elements is multiplied by the filter coefficients and the set is summed to one output line.

DESCRIPTION OF THE INVENTION

FIG. 1*a* illustrates the filter kernel of a bilinear interpolation filter;

FIGS. 1*b* and 1*c* illustrate the frequency response of a bilinear interpolation filter with 3 to 4 scaling; and

FIG. 1*d* illustrates the aperture effect;

FIG. 2 is an overall block diagram of a video display system;

FIG. 3 is a flow chart of the method according to the present invention;

FIG. 4*a* illustrates an ideal frequency response for a 3 to 4 scale filter;

FIG. 4*b* illustrates an optimal frequency response;

FIG. 5 illustrates how the delays and coefficients are operated on to achieve the desired line output in a vertical scaling function;

FIG. 6 illustrates frequency domain responses of the bilinear filter of the prior art (FIG. 6*a*) and two new scaling filters with a first filter with 4 taps (FIG. 6*b*) and a second filter with 6 taps (FIG. 6*c*).

FIG. 7*a* illustrates filter kernel coefficients for bilinear filter of prior art;

FIG. 7*b* illustrates the first filter coefficients;

FIG. 7*c* illustrates the second filter coefficients;

FIGS. 8*a* and 8*b* illustrates 3 to 4 scaling coefficients applied using first filter; and

FIG. 9 illustrates the scaling results of bilinear filter (9*a*), first filter (9*b*), and second filter (9*c*) for 3 to 4 scaling.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to FIG. 2, there is illustrated a video display system using the image scaling filters in accordance with the present invention. A video source 11, which may be from a cable, a VCR, or some other source, is applied through the A/D (analog-to-digital) converter 13 and the digital representation of the video signal which includes signal decoding at signal processor 14 to convert from decoded composite to luminance Y and chrominance C (I & Q) signals whether it be interlaced or non-interlaced depending upon the application. The output Y and C is applied through a scaling filter 15, which in turn may be applied through a color-space conversion 16 through a digital to analog (D/A) converter 16*a* to a CRT 17, or directly applied from conversion 16 to a display such as a digital mirror device (DMD) display 18, which was described in a 1987 article by Larry J. Hornbeck, a Texas Instrument Inc. scientist and described for example in the November issue of *The Institute of Electrical and Electronic Engineers Spectrum*, pages 27–31. In some cases, the scaling may be done after the color-space conversion. In the case of a VGA input, no color-space conversion is used. The video signals may be digital, in which case there is no analog-to-digital conversion. The input digital signals may also be non-video imagery digital signals from a photographic or printing device, and the picture elements from these are to be scaled up (increasing picture size) or scaled down (decreasing picture size).

Referring to FIG. 3, there is illustrated a flow chart for the method of the present invention for designing optimal scaling filters to overcome the problems explained in the Background of the Invention Section. The first step 101 is to determine the ideal frequency response. FIG. 1*b* illustrates by the heavy line marked "ideal" identifies for the 3 to 4 scaling the ideal frequency response. This ideal frequency

response eliminates aliasing while at the same time reducing the aperture effect. However, such ideal frequency response with abrupt cutoff cannot be realized in practice.

FIG. 4a, there is illustrated another ideal frequency response for a 3 to 4 scale filter. The zero crossing of that signal changes for each scale factor. The ideal frequency response, however, has a response that goes on for infinity and also cannot be realized in practice. In accordance with the present invention, for a given scale factor Applicant's invention computes first the ideal frequency response and then uses that in step **102** to estimate a desired optimal frequency response. Computation of optimal frequency response from ideal frequency response is an iterative process. Different numbers of filter taps and smoothings are tried and in each iteration the difference between the optimal and actual frequency response is measured. This process is iterated until the optimal and ideal response are close to each other (within acceptable bound of tolerance). The optimal frequency response is done by smoothing depending upon how many filter taps. FIG. 4b illustrates the smoothing estimate of FIG. 4a. Once this smoothing estimate is determined, then it is fed into a filter design algorithm (such as the Parks-McClellan algorithm) in step **103**, along with the desired number of filter taps. The Parks-McClellan algorithm is commercially available (e.g., as part of the MATLAB software package). The MathWorks, Inc., Cochituate Place, 24 Prime Parkway, Natick, Mass. 01760.

The Parks-McClellan FIR filter design algorithm is perhaps the most popular and widely used FIR filter design methodology. In the Signal Processing Toolbox, the function called remez designs linear phase FIR filters using the Parks-McClellan algorithm. The Parks-McClellan algorithm uses the Remez exchange algorithm and Chebyshev approximation theory to design filters with optimal fits between the desired and actual frequency responses. The filters are optimal in the sense that the maximum error between the desired frequency response and the actual frequency response is minimized. Filters designed this way exhibit an equiripple behavior in their frequency response, and hence are sometimes called equiripple filters.

The function

b=remez (n, f, m)

returns row vector b containing the n+1 coefficients of the order in FIR filter whose frequency-magnitude characteristics match those given by vectors f and m. Vectors f and m specify the frequency-magnitude characteristics of the filter:

- f is a vector of frequency points, specified in the range between 0 and 1, where 1.0 corresponds to half the sample frequency (the Nyquist frequency).
- m is a vector containing the desired magnitude response at the points specified in f. The elements of m must appear in equal-valued pairs.
- f and m must be the same length. The length must be an even number.
- The first point of f must be 0 and the last point 1.
- The frequencies must be in increasing order.
- Duplicate frequency points are allowed, but remez will separate them by 0.1 if they are exactly coincident. Note that frequency transitions much faster than 0.1 are undesirable because they can cause large amounts of ripple in the magnitude response.

plot (f,m) can be used to display the filter shape.

The number of filter taps directly impacts the cost of the real-time implementation of the filter. The filter design algorithm computes the set of multiplier coefficients to match with the number of taps in the optimal frequency response. The coefficients are collected or binned into sets for a given output line in step **104**. The coefficient sets (step **105**) are rescaled so for each set so the sum of the coefficients equals one (1). The input lines are multiplied and summed in step **106** to provide the values on the output lines. FIG. 5 illustrates a four tap filter for scaling. The four input lines are multiplied by the four coefficients at the four multipliers **41** and summed at summer **43**. The four inputs are separated by the line delays **45**.

FIGS. 6b and 6c illustrate the frequency domain responses of two scaling filters designed using this method of 3 to 4 scaling. These filters are referred to as Filters **1** and **2**, respectively. Filter **1** (FIG. 6b) has 4 taps per line, while Filter **2** (FIG. 6c) has 6 taps per line. The frequency response of bilinear filter is shown in FIG. 6a for comparison. The hatched portion of each frequency response corresponds to the aliasing region.

FIG. 7 illustrates the filter kernels for bilinear interpolation (FIG. 7a), Filter 1 (FIG. 7b), and Filter 2 (FIG. 7c). Referring to FIG. 7a, there is illustrated the bilinear interpolation according to the prior art with the coefficients illustrated at two taps per line. There are seven coefficients, with the first and seventh coefficient being at 0.25, the second and sixth coefficient being at 0.50, the fourth coefficient being at the peak at the coefficient at 1.0, and coefficients three and five being at 0.75. In accordance with Applicant's invention shown in FIG. 7b, the Filter 1 with four taps per line has **15** coefficients with the values indicated ranging on both the first and the fifteenth being −0.0019 and having a maximum value of 0.25 at the eighth coefficient. The first coefficient is binned with the fifth, the ninth, and the thirteenth, which binned set then corresponds to a coefficient set for a given output line. FIG. 7b illustrates the sixteen coefficients for four taps per line for a 3 to 4 scaling filter. The number shown in the figure is the output from the filter design algorithm. As discussed previously, Applicant's method then decodes these numbers into a format suitable for actually implementing scaling filters. Thus the output of the filter design algorithm, which consists of the following set of numbers [−0.0019, −0.0077, −0.0128, 0.0, 0.0494, 0.1327, 0.2152, 0.25, 0.2152, 0.1327, 0.0494, 0.0, −0.0128, −0.0077, and −0.0019] are binned into the following sets, each set corresponding to a coefficient set (one coefficient for each input line) for an output line:

[−0,0019,0.0494,0.2152,−0.0128], [−0.0077,0.1327, 0.1327,−0.0077],

[−0,0128,0.2152,0.0494,−0.0019], [0.0,0.25,0.0].

Since there are four taps per output line, every fourth coefficient represents the coefficient for the adjacent line.

These coefficient sets are then rescaled so that each set sums to one and the resulting values are applied to the multiplier **41** as shown in FIG.5 and as shown in FIG. **8**.

As illustrated in FIG. 7c, there is illustrated a design filter with six taps per output line with twenty-four different coefficients ranging from 0 to a maximum of 0.2 at the mid-point of coefficient **12**. In that embodiment there would be six coefficients (six lines) for a given output line, and these coefficients would again be rescaled so that the set sums to 1. These scaled coefficients are the multiplier values in FIG. 5. FIG. **8** shows 3 to 4 scaling realization using Filter **1**.

Referring to FIG. 8a, there is illustrated how the samplings would be applied to the lines in the 3 to 4 scaling. If an input line is directly in line with the output line as line **0** to **0'**, then it would be a 1 to 1 relationship. If not, Filter **1**

with 4 taps would have the coefficient of −0.8611 from input line 1 to output line 1,' and the coefficients of -7.6×10^{-3} between input line −1 and output line 1', 0.197 from input line 0 to output line 1', and −0.0512 from input line 2 to output line 1'. These input line coefficients would sum up to the total sum of 1. These would be scaled from the coefficients represented by the Filter 1. This would represent for example the first set for the first output line, the second set would follow the next set of coefficients as binned for the second output line, the third output line would be the third set of coefficients binned, and the fourth output line be the fourth set or bin. Thereafter, it would repeat going back to the first set or bin, second, third, and then the fourth set or bin for the fifth, sixth, seventh, and eighth output lines.

FIG. 8*b* also shows the 3 to 4 scaling for Filter 1, for output line 2' taken from line 0, 1, 2, and 3 with the coefficients being −0.0308, for input line 0, 0.05308 for lines 1 and 2, and −0.0308 for line 3. All of these coefficients would be rescaled to sum to 1 and that value would become the multipliers for the corresponding input line with the lines being appropriately delayed as summed as illustrated in FIG. 5 to derive the output value for line 2'. Similarly the input to output line 3' from input lines 1, 2, 3, and 4 would have the coefficients indicated as −0.0512 from line 1, 0.8611 from line 2, 0.1977 from line 3, and -7.6×10^{-3} from line 4.

Filter in FIG. 7*b* is:

[−0.0019, −0.0077, −0.0128, 0.0, 0.0494, 0.1327, 0.2152, 0.25, 0.2152, 0.1327, 0.0494, 0.0, −0.0128, −0.0077, −0.0019]

This is binned into:

A=[−0.0019, 0.0494, 0.2152, −0.0128]

B=[−0.0077, 0.1327, 0.1327, −0.0077]

C=[−0.0128, 0.2152, 0.0494, −0.0019]

D=[−0.0, 0 0.25, 0.0]

Elements of A sum to:

−0.0019 +0.0494+0.2152−0.0128=0.2499

dividing each element of A by this,

$$\left[\frac{-0.0019}{0.2499}, \frac{0.0494}{0.2499}, \frac{0.2152}{0.2499}, \frac{-0.0128}{0.2499}\right]$$

$=[-7.6\times10^{-3}, 0.1977, 0.8611, -0.0512]$

FIG. 9 shows the scaling results of bilinear (FIG. 9*a*), Filter 1 (FIG. 9*b*), and 2 (FIG. 9*c*) for 3 to 4 scaling on a circular zone plate. This is a standard test used to evaluate interpolation algorithms. Note the significant aliasing in the top picture with bilinear interpolation in FIG. 9*a*. The improvement with Filter 1 (FIG. 9*b*) and almost complete elimination of aliasing with Filter 2 (FIG. 9*c*).

The above scaling is vertical scaling by changing the number of horizontal lines. This scaling can also be applied to width scaling by changing the number of pixels (picture elements) per line and using adjacent pixels. FIG. 2 would have pixel delays rather than line delays. The steps in FIG. 3 of starting with an ideal frequency response and converting to an optimum frequency response by a smoothing estimation would be done. The filter coefficients would then be determined based on the number of taps per line. The coefficients are then binned and rescaled to equal one. The adjacent input pixels are multiplied by the coefficients and are summed to get the new output pixel.

What is claimed is:

1. A method of forming an optimal image scaling filter for converting a first number of input pixels to a second number of output pixels comprising the steps of:

determining an ideal frequency response for a given scaling factor;

determining from an ideal frequency response a smoothing optimal frequency response with a determined number of taps;

generating filter coefficients based on the determined number of filter taps and the optimal frequency response;

binning said coefficients into a set corresponding to the closest input pixels to said output pixel;

rescaling said coefficients in said set so that each said set sums to one;

multiplying the closest input pixels to an output pixel according to said rescaled coefficients in said set; and

summing said multiplied input pixels in said set to achieve the output pixel value.

2. The method of claim 1 wherein said generating step includes using Parks-McClellan algorithm.

3. The method of claim 1 wherein said input pixels are on adjacent input lines and said output pixel is on a closest output line.

4. The method of claim 3 wherein said generating step includes using Parks-McClellan algorithm.

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